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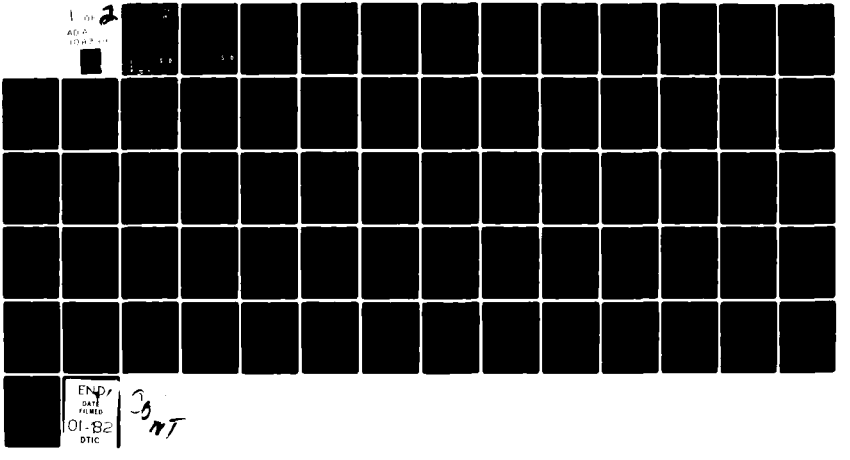

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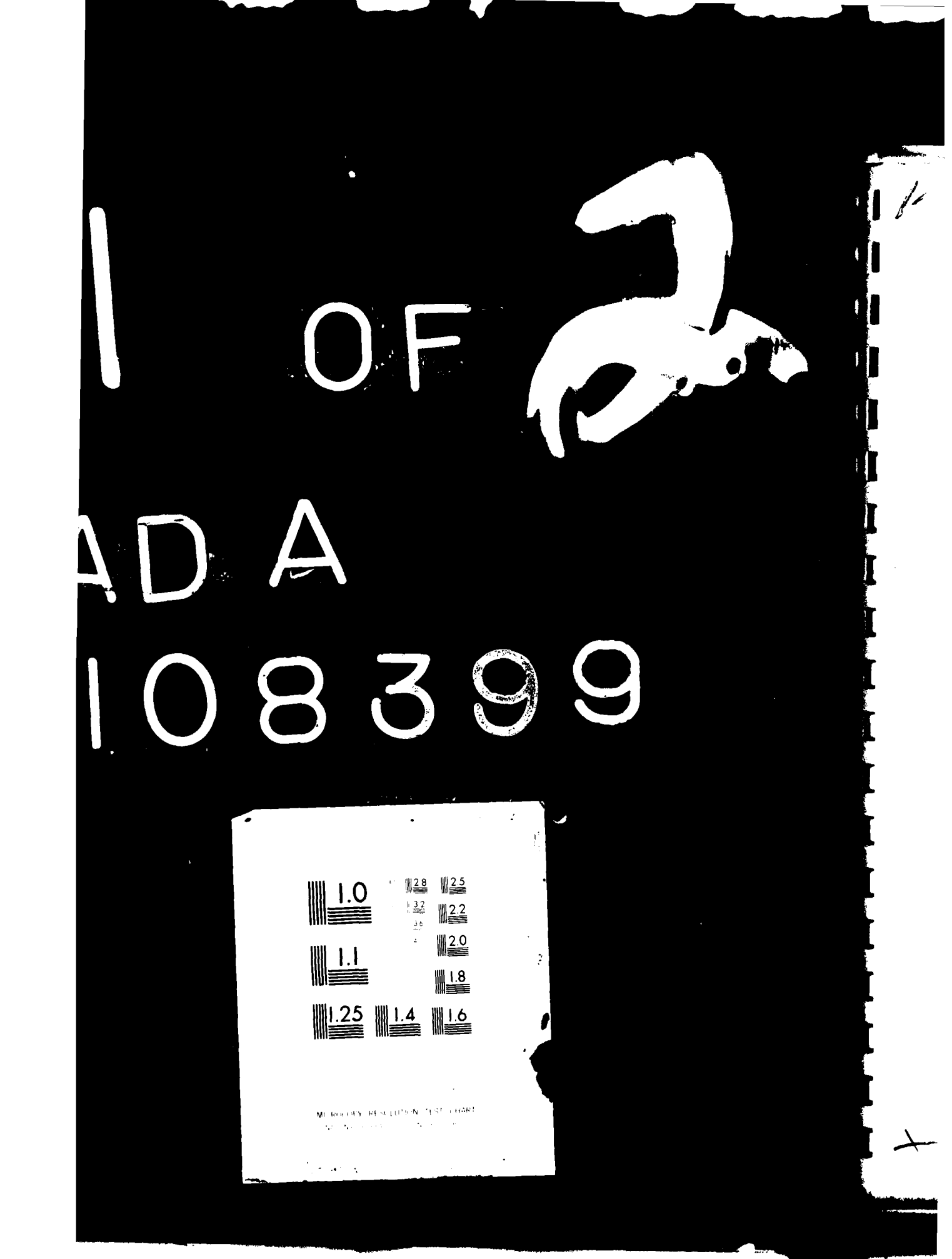
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LEVEL II

FIVE YEAR TECHNICAL REPORT
3/1/77 - 4/30/81
CORNELL UNIVERSITY
CONTRACT #F49620-80-C-0069

MICROWAVE SEMICONDUCTOR RESEARCH -- MATERIALS, DEVICES, CIRCUITS

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FIVE YEAR TECHNICAL REPORT

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MATERIALS, DEVICES, CIRCUITS

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The growth and characterization of high purity and chromium doped GaAs and Al,GaAs for buffer layers in high performance GaAs FET's has been carried out. Deep level transient spectroscopy has been used to measure electron traps in Schottky diodes and GaAs FET's.

The investigation of microwave field-effect transistor performance limits set by layer composition and contact geometry has been carried out. The

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several critical physical electronics parameters for very high voltage operation of GaAs power FET's have been determined. The electric field distribution and the parasitic output conductance due to buffer layer current were studied and optimized.

The use of MBE tailored doping profiles for improved microwave device operation has been studied. Improved linearity of GaAs power FET devices and the optimization of doping planes for potential barriers and other purposes were also carried out.

GaAs/Al,GaAs selectively doped heterojunctions were grown by MBE and were studied for potential use in high performance transistors. High electron mobility (80.000 cm^2/v-s) at 77°K was first obtained in this effort, following the optimization of the growth conditions of the Al,GaAs. In addition, high resistivity Al,GaAs buffer layers for power FET's were obtained.

Two dimensional computer simulations of FET devices in various materials were also made. Some techniques for reducing leakage in Schottky barriers on low-band-gap material were investigated.

Fundamental design studies for GaAs FET integrated circuits were carried out using a computer. Matching networks for optimisized gain or noise figures, across bread bands, were determined.

A new method of broadband circuit design which does not require device equivalent circuit determination, has also been studied, and some particular examples have been optimized.

The dynamic and spectral characteristics of semiconductor laser materials and structures have been investigated. Several specific laser systems, including external components are included.

High speed optical receivers for optical communications were investigated. New high speed detectors using GaAs and In,GaAs were constructed and tested.

A project to construct MOCVD equipment for compound semiconductor growth has also been underway, in order to complement the MBE and LPE methods already developed.

TABLE OF CONTENTS

TABLE OF CONTENTS (CONTINUED)

L.F. EASTMAN and D.W. WOODARD

5/1/77 - 4/30/81

TITLE: **GROWTH AND CHARACTERIZATION OF GaAs FOR HIGH PERFORMANCE MICROWAVE DEVICES**

Objectives

Overall objectives are improved GaAs epitaxial materials for microwave devices and further understanding of substrate properties and their relation to interface and epitaxial layer properties. The approach taken has been to grow high purity buffer layers by LPE with high precision and reproducibility, to develope means to quantitatively measure the Cr content and characterize the semi-insulating mechanisms, and to explore the properties of FET devices and how these depend on characteristics of the buffer layer. Both GaAs and $Al_xGa_{1-x}As$ buffer layers have been investigated in the program.

Progress

Background Purity in LPE Growths

During this program, melt contamination by atmospheric impurities during furnace loading was investigated. Such contamination can be purged by baking at growth temperature for up to 24 hours prior to each growth. However, the consequences of such baking are reduced throughput and increased surface degradation of the substrate. It was found tht the amount of contamination is related to the surface area and number of mating surfaces on the graphite growth boat, and is unrealted to exposure of the melt surface to the atmosphere. Two coatings for the graphite-pyrolytic and surface densification by Ultra Carbon, Inc. EXU process - were investigated and found not to produce significant improvement. A boat of very small and simple design was found to yield almost contamination free growth after less than 1 hour of purging. A more complex boat with a number of mating surfaces produced growths with contaminats in the low 10^{15} range after a similar purging time. A glove box flushed with nitrogen direct from a cylinder (no additional purification) was found to be sufficient to prevent the contamination when employed to prevent exposure of the boat to ambient air during loading.

Standard procedure for achieving a limiting background purity in the range 1 to 2 x 10^{14} ionized impurities per cm^3 is thus the following: (1) any new graphite boat is induction heated under high vacuum for 1 to 2 hours at 1200 to 1400°C in a water cooled quartz chamber. Following this, the new boat is baked at 1000°C for 15 hours in flowing, ultra pure H_2; (2) any new melt is baked in H_2 at the intended growth temperature for a time which depends on that temperature. For optimum purity 700°C is employed for growth temperature and the baking time required is 24 hours. At higher growth and baking temperatures shorter times are required to reach the limiting purity but higher limits of background (silicon) impurities will result; (3) melts used for repeated growths must be baked again at growth temperature after each time the furnace is opened, to remove contaminants absorbed by the graphite during the opening. The extent of this bake depends on the boat design and the efficacy of the glove box, if any, which is employed to exclude air during loading.

Chromium Doping

The distribution coefficient and solubility limit of Cr were measured at four different growth temperatures between 700 and 850°C using measurement techniques to be described below. The previously reported presence of a shallow donor impurity species included in the highest available purity Cr was confirmed. This impurity can be purged by pre-baking Cr doped melts at 900°C for 10 hours, but at such temperature, high concentrations of Si impurities are introduced to the melt as a consequence of higher quartz dissociation rates. The time required to re-equilibrate the Si concentration in the melt to the purity limit for growth at 700°C was measured and found to be 72 hours. Shorter times could be expected at higher growth temperatures, but have not been measured. For growth above 700°C Cr doped melts were first baked for 10 hours at 900°C and subsequently were re-equilibrated to the purity limit by baking for 72 hours at 700°C before substrate loading. After substrate loading, the system was baked at growth temperature as described in the previous section relating to atmospheric contamination. It is to be noted that only the latter, post loading, bake needs to be done in the growth reactor. The additional baking required to control the Cr-included impurities can be done in a separate furnace capable of

handling multiple melts simultaneously, so that useable growth reactor time need not be consumed by prolonged baking cycles.

Measurement of Cr Concentration

In order to confirm that the above purification and Cr doping techniques result in a single Cr deep acceptor and to measure its concentration as a function of growth conditions, Hall effect and DLTS measurements were made on Cr doped material which was made conducting, either n or p type, by simultaneously doping with either Sn or Ge respectively. In n type material the amount of compensation and total ionized impurity concentration resulting from addition of Cr to the melt was measured by Hall effect. In the same material the Cr deep acceptor concentration was measured by optical DLTS. Comparison revealed good agreement between compensation, deep acceptor concentration, and increase of total ion concentration all resulting from Cr additions. This confirmed the validity of the DLTS technique as a sensitive probe of Cr deep acceptor concentration and demonstrated that the above purging procedures are sufficient to elliminate the extraneous energy levels which are otherwise introduced by Cr doping at LPE temperatures.

The use of optical DLTS for quantitative measurement of the Cr deep acceptor concentration required knowledge of the ratio

$$\frac{e_p^{\,o}}{e_p^{\,o}+e_n^{\,o}}$$

where $e_p^{\,o}$ and $e_n^{\,o}$ are the optical emission rates, for holes and electrons respectively, at the wavelength employed. This was obtained by electrical DLTS measurement of the Cr deep acceptor concentration in p type material where the level is readily apparent as a hole trap. The optical emission ratio could then be obtained by optical DLTS in the same material. Since the emission ratio is independent of conductivity type, the result was then applied to the Cr measurements in n type material.

Buffer Layer Studies

With knowledge of purification procedures and Cr doping effects obtained as described above, high purity semi-insulating GaAs and

$Al_xGa_{1-x}As$ buffer layers with predictable Cr concentrations from 0 to 6 x $10^{15}/cm^3$ were grown at temperatures not exceeding 850°C. Using doped active layers also grown by LPE the properties of FET devices were measured as functions of the buffer layer composition and Cr doping. In GaAs buffer layers the parasitic dc output conductance was found to decrease when the Cr concentration exceeded 5 x 10^{15}. In $Al_{.3}Ga_{.7}As$, reduced output conductance was observed at all Cr concentrations including zero. These results provided support for the Eastman and Shur model of injected space charge parasitic current in the substrate (or buffer), which support was previously lacking since in bulk material, both Cr doped and undoped, the deep level density generally exceeds 5 x 10^{15} while in buffer layers grown by other techniques the Cr and other deep level concentrations are not precisely known.

Field Dependence of the Cr Emission Rate

The high purity and complete absence of the EL-2 level in the Cr doped LPE material achieved under this program made it ideal for studies of field dependence of the electron emission rate, e_u, of the Cr deep acceptor level, which studies were being attempted by researchers at LEP in France. Working in collaboration, to provide LEP with samples of material having the requisite properties, it was found that at field strengths of 2 x 10^5 v/cm typically existing in power FET structures, e_n is 10^{15} times greater than the low field value. This result has serious consequences for the use of ion implantation into Cr doped substrates for power FET's. Similar effects have also been observed at LEP for the EL-2 level common to bulk semi-insulating material meaning that for power FET's, best results can only be achieved in substrate material with low Cr and EL-2 concentrations.

Deep Levels Introduced by Ion Implantation

Working in collaboration with Westinghouse Research Laboratories, the deep level concentrations in implantedlayers in bulk substrates and high purity LPE material were compared. It was found that under cap and anneal conditions the concentration was very low in the LPE material meaning that most deep levels in implanted layers are due only to the substrate and not the implant. Material implanted through a silicon nitride cap was found to contain copper indicating that for this process, care must be taken to avoid Cr contamination in the nitride

deposition chamber.

Deep Level Diffusion From Substrate Into Epitaxial Layers

Work was done which shows that the diffusion of deep levels from substrates into active layers during anneal at 800°C can be greatly reduced by pre-annealing the substrates in flowing H_2 for 16 hours at 780 and then etching 1 micron or more from the surface prior to active layer growth. It was also found that the LPE purification bake of 24 hours at 710° is not sufficient to reduce the deep level concentration. Epitaxial layers doped at 10^{17} and several microns thick were found to be almost completely compensated after an anneal at 800°C for 1/2 hour if the substrates were not annealed at 780° prior to growth. This occurred even where the substrate was subjected to the 710, 24 hour bake, but did not occur after the 780° prebake.

Publications

1. "Domain Formation in MESFETs - Effects of Device Structure and Materials Parameters", S. Tiwari, D. W. Woodard and L. F. Eastman, 7th Biennial Cornell Conf. on Microwave Semiconductor Devices Circuits (Aug. 1979).

2. "Surface and Interface Depletion Effects on High Purity GaAs Buffer Layers", A. Chandra, C. E. C. Wood, D. W. Woodard and L. F. Eastman, PCSI 8, Williamsburg, VA (Jan. 1981).

3. "Detailed Electrical Characterization of the Deep Cr Acceptor in GaAs", G. M. Martin, A. Mittoneau, D. Pons, A. Mircea, and D. W. Woodard, J. Phys. C. Solid State Physics, 13, p. 3855 (1980).

4. "Substrate Current in GaAs MESFETs", L. F. Eastman and M. S. Shur, IEEE Trans. on Electron. Devices, ED-26, p. 1359 (1979).

5. "Effects of Ion Implantation on Deep Levels in GaAs", T. R. Jervis, D. W. Woodard, L. F. Eastman, Electronics Letters, Vol. 15, No. 20, p. 619 (Sept. 1979).

6. "Phonon Assisted Tunnel Emission of Electrons from the Cr Level in GaAs", S. Makram-Ebid, G. M. Martin and D. W. Woodard, Proc. 15th International Conference on the Physics of Semiconductors, Kyoto, Sept. 1980, to be published by the Institute of Physics Conference Series, London.

7. "Investigation of Deep Levels in GaAs MESFETs Introduced by Device Processing", G. N. Maracas, J. G. Tenedorio and L. F. Eastman, 8th Biennial Conf. on Active Microwave Semiconductor Devices and Circuits, Cornell University, Ithaca, NY (Aug. 1981).

8. "The Analysis of Exponential and Nonexponential Waveforms in Deep Level Transient Spectroscopy", P. D. Kirchner, W. J. Schaff, G. N. Maracas and L. F. Eastman, 8th Biennial Conf. on Active Microwave Semiconductor Devices and Circuits, Cornell University, Ithaca, NY (Aug. 1981).

9. "Study of High Purity and Semi-Insulating $Ga_{1-x}Al_xAs$ ($x < 0.45$) Buffer Layers for High Performance FET's", S. Tiwari, M. G. Spencer, L. F. Eastman and D. W. Woodard, 8th Int. Symp. on GaAs and Related Compounds, Vienna (Sept. 1980).

Thesis

D. W. Woodard - May 1979

G. Maracas - January 1982

Talks

1. "Cr Doped GaAs Grown by Liquid Phase Epitaxy", D. W. Woodard, IEEE Workshop on Compound Semiconductor Microwave Devices, San Francisco, CA (Feb. 1978).

2. "Cr Doped Semi-Insulating GaAs Buffer Layers for FET's Grown by LPE", D. W. Woodard and L. F. Eastman, IEEE Workshop on Compound Semiconductor Microwave Devices, San Francisco, CA (Feb. 1978).

3. "The Use of $Al_xGa_{1-x}As$ Buffer Layers to Reduce Parasitic Space Charge Limited Current Flow Through the Substrate in FET Structures", L. F. Eastman, D. W. Woodard, a. Chandra and M. Shur, IEEE Workshop on Compound Semiconductor Microwave Devices, San Francisco, CA (Feb. 1978).

4. "Growth and Assessment of High Purity Cr Doped Buffer Layers for High Performance Devices", D. W. Woodard, U.S./France Workshop on Microstructures and GaAs High Performace Devices, Gif-sur-Yvette, France (Nov. 1979).

5. "Solubility and Distribution Coefficient of Chromium in GaAs Grown by Liquid Phase Epitaxy", D. W. Woodard, P. D. Kirchner, W. J. Schaff, S. Tiwari, R. Stall and L. F. Eastman, Conference Serie Number 56, The Institute of Physics, London, p. 83 (1980).

6. "Phonon Assisted Tunnel Emission of Electrons From the Cr Level in GaAs", S. Makram-Ebeid, G. M. Martin and D. W. Woodard, Int. Conf. on the Physics of Semiconductors, Kyoto, Japan (Sept. 1980).

7. "Growth by LPE and Characterization of High Purity Cr Doped GaAs", D. W. Woodard, Invited paper at 5th Int. Conf. on Vapor Growth and Epitaxy in Conjunction with 5th American Conf. on Crystal Growth, San Diego, CA (July 1981).

Seminars

Hughes (Malibu), Hughes (Torrance), Varian, Honeywell, NRL, Notre Dame, Research Triangle Institute, U. Michigan, Wayne State, Columbia, Duke, U. Illinois, Pittsburgh U.

Technology Transfer

1. Cr. Doped Buffers Technology transferred to Honeywell.
2. Cr Doped LPE Technology transferred to Narda Microwave Corp.
3. High Purity AlGaAs and InGaAs transferred to Bell Telephone Labs.

4. Material Sent to Narda for Device Evaluations.
5. Material sent to IBM for Implantation Evaluation.
6. LPE material used at Westinghouse to test deep levels from ion implantation.
7. Technology of high purity LPE GaAs transfer to General Electric.

Personnel

L. F. Eastman
D. W. Woodard
G. Maracas
S. Tiwari
J. Tenedorio

L.F. EASTMAN and D.W. WOODARD

5/1/77 - 4/30/81

TITLE: **INVESTIGATION OF MICROWAVE FIELD-EFFECT TRANSISTOR PERFORMANCE LIMITS SET BY LAYER COMPOSITION AND CONTACT GEOMETRY**

Objectives

The objective of this task has been to investigate experimentally and analytically the performance limits of GaAs microwave power FET devices. The approach taken has been to explore structural and materials related determinants of the breakdown voltage and output conductance. Surface field profile in the channel was studied by electron beam induced current and also by scanning auger microprobe analysis of the energy shift of auger peaks originating from incidental carbon surface contaminants.

Progress

The period of this report covers the research activity at Cornell in power FET's and micron sized GaAs devices, in general, from its inception. During this time technology for fabrication of 1 micron GaAs devices by projection optical lithography was acquired, and power FET structures with the highest reported breakdown voltages were achieved. 85 volts from drain to source at pinch-off condition was found to be possible for devices having 5 V pinch-off voltage. At full channel current the breakdown voltage was reduced to 60 v, but this bias condition need never be realized in normal operation.

The optimized critical design parameters for the X-band device were found to be:

1. Thickness of pure GaAs (or $Al_{.35}Ga_{.65}As$) buffer layers must be greater than 1 μm. Undesired output conductance rose nearly linearly with buffer layer thickness, so no more than 3 μm was used.
2. Doping of GaAs active layer for this operating frequency should be about $8 \times 10^{16}/cm^3$. Lower breakdown voltages occurred for lower or higher dopping, although larger

donor concentration had a more gradual reduction of breakdown voltage.

3. The product of the doping density times the active layer thickness under the gate should be 2 x $10^{12}/cm^2$ or a little less, yielding .33A of full channel current or less per millimeter width of gate. The drain to gate breakdown voltage is nearly reciprocally related to this product.
4. The gate should be recessed by an amount equal to the surface charge depletion in the unmetallized portion of the channel. The .6V band bending usually encountered yields .1 μm depletion at free channel surfaces, so the channel not under the gate should be .1 μm thicker than that under the gate. The use of an anisotropic etch to make the gate notch is desired, so that the radius of curvature of the gate metal deposited is ~.1 μm where it fills in the etch notch. The elimination of excessive fields, and even moving Gunn domains along the channel, are prevented at full channel current by this aspect of the design.
5. The channel thickness under the source and drain contacts should be twice as big as that under the gate. To etch the notch for the total length of the channel, an anisotropic etch should again be used to round the ends. Current crowding and breakdown at the drain is prevented by this design.
6. The gate should have a moderately large separation from the drain, while having a small separation from the source. A value of 4.5 μm or more between gate and drain, but only 1.0 μm between gate and source, are required for best operation.
7. The use of thin N^+ contact layers on top of the thickest part of the channel is recommended, although it was not found to be essential. What is essential, however, is the separation of the drain contact metal from the location of the start of this thickest part of the channel. About

1 μm separation should suffice.

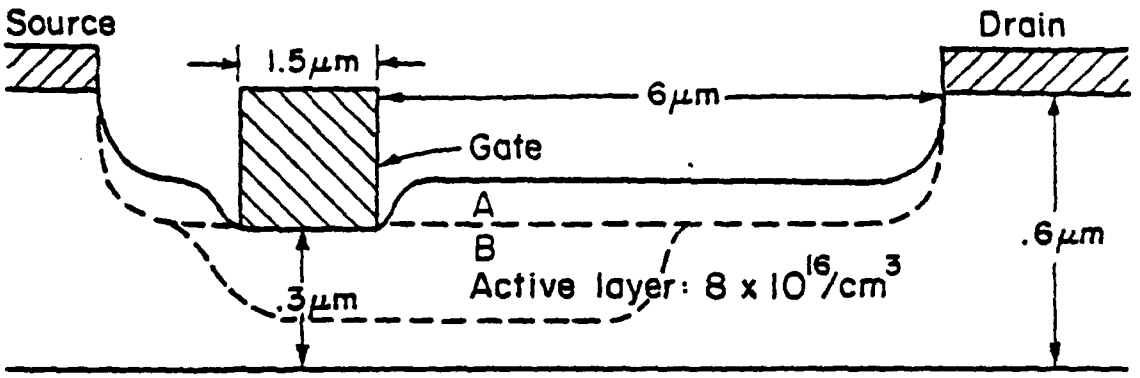
8. Finally, the surface oxide should be (gently) removed in a H_2 plasma and Si_3N_4 should be (plasma) deposited on the channel surface as passivation, in order to yield reliability.

Figure 1 summarizes the parameters of a high breakdown voltage device designed in accordance with the foregoing, and shows a profile of the electric field determined from scanning auger microprobe analysis in the gate-to-drain portion of the channel.

Using the simple parabolic functional form for the stationary high field domain that naturally forms on the drain side of the gate, (1) and a hot electron diffusion constant of 50 $cm^2/v.sec.$, the strength and thickness of the field peak shown. This figure was predicted to be 250 hv/cm and 2.8 μm respectively, in good agreement with the experimental result. From electron and hole avalanche coefficients in the (110) and especially in the (100) directions (2) such a domain was found to be sustainable without breakdown. The gate to drain spacing must thus be sufficient to allow this domain to form undistorted to prevent further increase of the field.

In Figure 2 the dependence of breakdown voltage on drain current is shown for a finger of 75 μm width, and channel design similar to Figure 1.

In addition to breakdown voltage, the normalized output resistance of power transistors was studied and improved. Higher values of this parameter are needed to maintain efficiency at higher operating bias. Both dc and microwave dissipation in the parasitic space charge limited current through the buffer and substrate prevent high efficiency at high bias and high frequency. The usual values of this parameter range from 150-300 Ω-mm. Using both undoped and lightly ($4 \times 10^{14}/cm^3$) chromium doped buffer layers, 2 μm thick, values of 600 Ω-mm of output resistance were obtained. The buffer layers used were developed on another task of this program. Our theoretical work predicted about 5% as many electrons injected into the buffer layer as there are electrons in the active channel. Thus about $4 \times 10^{15}/cm^3$ injected electrons are



(1a) Power FET Cross Section

Depletion Region

Case A: Low Drain Voltage, Forward Gate Bias

Case B: High Drain Voltage, Negative Gate Bias

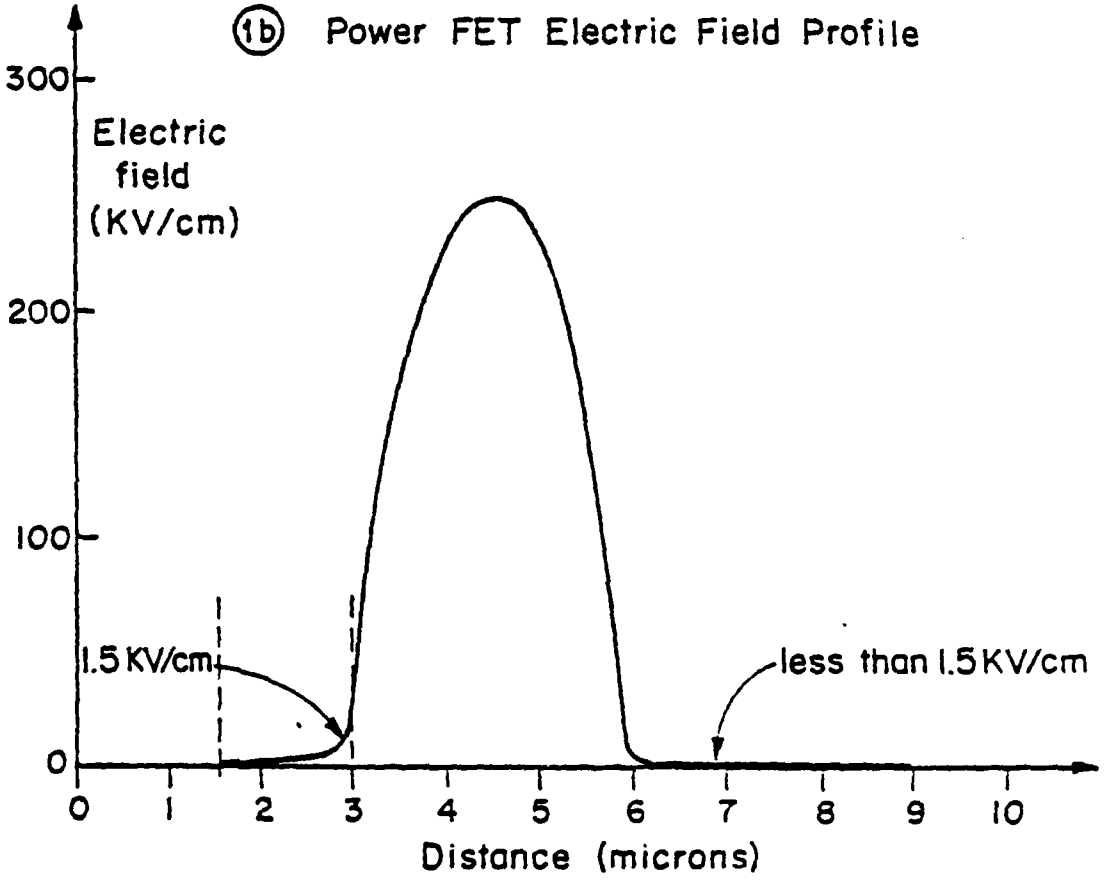


Figure 1 - Power FET Structure

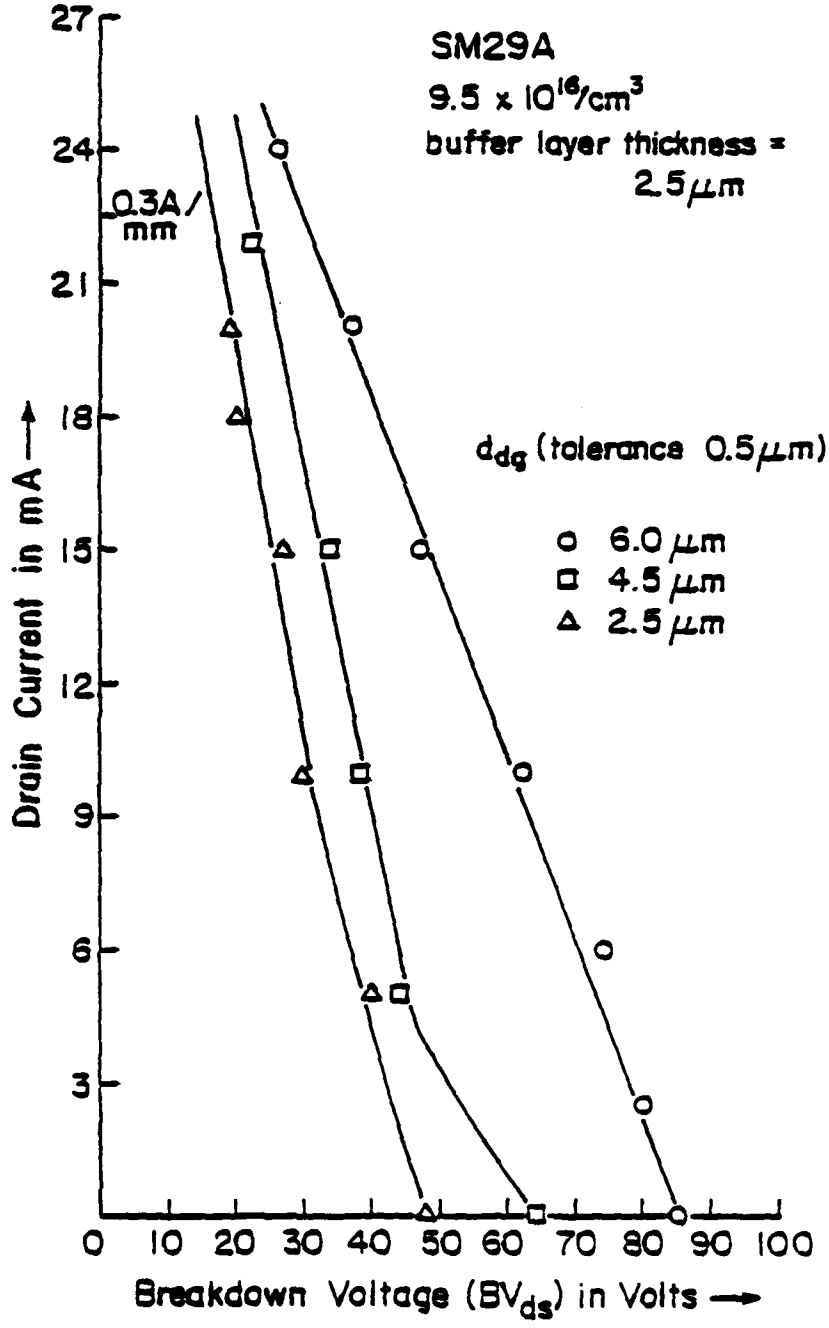


Figure 2. Burnout Voltage as a Function of Channel Current and Drain to Gate Spacing, Doping = 9.5×10^{16} cm^{-3}.

present, clearly many more than the chromium traps with light chromium doping. While successful chromium doping to 4 x $10^{15}/cm^3$ has been developed, it has now been determined that chromium traps lose their electrons in very high fields, so limited ranges of operating voltage must be expected when increased output resistance is obtained with heavy chromium doping.

The growth of $Al_{.4}Ga_{.6}As$ buffer layers, both undoped and lightly Cr-doped (4 x $10^{14}/cm^3$) were achieved. Such buffer layers were tried in power FET structures and yielded up to 1,6000 Ω-mm output resistance, a new state of the art. A key reason for the increased output resistance is the very low saturation velocity for electrons in high fields in $Al_{.4}Ga_{.6}As$. This saturation velocity is at least 2.5:1 lower than that in GaAs. Since the injected space charge magnitude and geometry will yield similar results in $Al_{.4}Ga_{.6}As$ buffers as in GaAs buffers, the current in the $Al_{.4}Ga_{.6}As$ is appropriately lower.

Publications on This Task

1. "Substrate Currents in GaAs FET's", L.F. Eastman and M. Shur, IEEE Transactions, Vol. ED-26, No. 9, pp. 1359-1362, Sept. 1979.
2. "Physical and Materials Limitations on Burnout Voltage of GaAs Power MESFETS", S. Tiwari, L.F. Eastman and L. Rathbun, IEEE Transaction, Vol. ED-27, No. 6, pp. 1045-1054, June 1980.
3. "Design Criteria for GaAs MESFET's Related to Stationary High Field Domains", L.F. Eastman, S. Tiwari and M. Shur, S.S. Electronics, Vol. 23, pp. 383-389, 1980.
4. "Domain Formation in MESFET's - Effects of Device Structure and Materials Parameter", S. Tiwari, D. Woodard and L.F. Eastman, Proc. IEEE Cornell Conf., Aug. 1980.
5. "The Study of High Purity and Semi-insulating $Al_{.4}Ga_{.6}As$ Grown by LPE", S. Tiwari, M.G. Spencer, H.M. Levy, S. Judaprawira, D.W. Woodard and L.F. Eastman, Proc. International Symposium on GaAs and Related Compounds, Vienna, Sept. 1980.
6. "Characteristics of Planar Doped FET Structures", K. Board, A. Chandra, C.E.C. Wood, S. Judaprawira and L.F. Eastman, IEEE J. Elec. Dev., ED-28 (5) 505 (May 1981).

Thesis on This Task

"A Study of the Device and Materials Related Aspects of the Microwave GaAs Power MESFET", S. Tiwari, Aug. 1980.

""Nonuniformly Doped Gallium Arsenide Microwave Power MESFETS", S. Judaprawira, May 1981.

Talks

"Use of AlGaAs Buffer Layers to Reduce Parasitic Space Charge Limited Current Flow Through Substrtes in FET Structures", L.F. Eastman, D.W. Woodard, A. Chandra and M.S. Shur, WOCSEMMAD, Atlanta, GA, Feb. 1979.

Publications on Related Projects

1. "The Liquid Phase Epitaxial Growth of High Purity $Al_xGa_{1-x}As$", A. Chandra and L.F. Eastman, J. Electrochem. Soc., Vol. 127, No. 1, pp. 211-216, Jan. 1980.
2. "A Study of Alloy Scattering in $Al_xGa_{1-x}As$", A. Chandra and L.F. Eastman, J. Appl. Phys., Vol. 51, No. 5, pp. 2669-2677, May 1980.
3. "A Study of the Conduction Properties of a Rectifying n-GaAs: n-$Al_xGa_{1-x}As$ Heterojunction", A. Chandra and L.F. Eastman, Solid State Elect., Vol. 23, pp. 599-603, 1980.

Information/Technology Transfer

Design and analysis of power GaAs FET's done for Westinghouse Research Lab.

Modelling of FET logic devices for Rockwell.

Modelling of FET logic devices for IBM.

Lincoln Labs.

Cooperative Design Processing, and testing of high power GaAs FET devices continuing with Westinghouse Research Laboratory. Effort on high breakdown voltage, high power, efficiency, frequency response.

Build-up of new large effort on GaAs power FET devices started at Microwave Associates by new Ph.D., Dr. S. Tiwari. Continuing cooperation on design and processing.

Transfer of design and processing techniques, to General Electric in Syracuse and Schenectady, on GaAs FET devices.

Transfer of GaAs Power FET design limit parameters, and critical comparison of breakdown results with Texas Instruments.

Transfer of GaAs power FET design limit parameters to Raytheon Research Laboratory.

Critical comparisons of GaAs power FET design limit parameters with Bell Laboratories.

Design, construction, testing and modeling of GaAs FET microwave and high speed logic devices on a joint program with IBM Federal Systems Division and Research Laboratory.

GaAs FET logic modeling program with Rockwell Science Center completed.

Personnel

L. F. Eastman
D. W. Woodard
S. Judaprawira
S. Tiwari
J. Tenedorio
A. Tenedorio

L. F. Eastman and C. E. C. WOOD

5/1/79 - 4/30/81

TITLE: **USE OF MBE TAILORED PROFILES FOR GaAs POWER FETs FOR IMPROVED PERFORMANCE**

On the subject of controling profiles for improved μ wave FETs we have investigated various buried channel approaches to improvement of linearity.

Predeposition of tin atoms prior to active layer epitaxy on undoped MBE GaAs buffers resulted in exponentially decreasing profiles with greatly improved DC transconductance linearity. Planar doping with Ge to form single crystal plane FETs was plagued by deep level concentrations which gave very poor gate-leakage characteristics and made it impossible to pinch devices off. DLTS studies are continuing to further understand this effect.

The deleterious effect of deep levels has been aleviated by spreading the (acceptor) plane over ~ 50-100 Å in the case of planar doped barriers. This is currently being tried with donor planes in FETs.

The use of n^+ contacts and non-alloyed Ge heterojunction contacts has been studied but hampered by a lack of refractory metal deposition equipment. This will be remedied in the near future as, in the second Cornell MBE machine there is an electron-beam-evaporator source and hearth.

Limits of doping concentrations have been studied for Si and Ge and Sn donor atom for n^+ contacts and work on Mg and Mn as acceptor species for planar-doped-barrier electron-confining buffer-layers have been initiated.

Initial results indicate the following $[Sn]_{max} \sim 3 \times 10^{19} cm^{-3}$. $[Si]_{max} \sim 6 \times 10^{18} cm^{-3}$, $[Ge]^n_{max} \sim 3 \times 10^{18} cm^3$. Ge is amphotenic and is therefore no longer used as a donor atom.

In the case of acceptors $[Mn]_{max} \sim 1.5 \times 10^{18} cm^{-3}$ and $[Mg]_{max} \sim 4 \times 10^{19} cm^{-3}$ however Mg has a very temperature dependant sticking coefficient. It now looks like Be will be the standard acceptor species for most III-V MBE compounds.

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Personnel

Masters Degree

D. DeSimone - May 1980

Ph.D. Degree

R. Stall - August 1980

G. Metze - May 1981

D. DeSimone - January 1982

L. F. Eastman and C. E. C. WOOD

5/1/79 - 4/30/81

TITLE: **MBE MULTIPLE GaAs - $Al_xGa_{1-x}As$ HETEROJUNCTIONS FOR CONFINEMENT OF ELECTRONS FOR IMPROVED FET PERFORMANCE**

The use of heterojunction buffer layers (AlGaAs) for GaAs FETs has been studied extensively by photoluminescence. Doped GaAs grown on AlGaAs was found to be electrically depleted and optically very poor quality unless the AlGaAs was grown in a very high vacuum condition, at very high temperatures (~700°C) and with a very limited $J_{As_4}/J_{(Ga+Al)}$ flux ratio. This result explained the inability of Rockwell, Thompson CSF, RSRE in England and others to improve performance of FETs.

FETs made here with AlGaAs buffers grown under partially optimised conditions gave a gain figure of 10 dB at 10 GHz with an output impedance of 2000 mm compared to 600 mm for GaAs buffered devices.

More recently studies in the area of modulation doping have been initiated.

μ_{77} figures in excess of 80,000 cm^2/vs have been obtained for multilayer structures and successful DC operation of a prototype two dimensional electron gas FET. Work is now in progress to improve ohmic contacts to the AlGaAs overlayers by non-alloyed Ge/AlGaAs ohmic contacts and by grading from AlGaAs to GaAs.

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7. "The Effect of Growth Conditions on Si Incorporation in MBE GaAS", Y.G. Chai, R. Chow and C.E.C. Wood, Appl. Phys. Lett. (Nov. 1981).

PERSONNEL

Ph.D. Degree

W-I Wang - January 1982

J. FREY

5/1/77 - 4/30/81

TITLE: **MATERIALS AND PROCESSES FOR MICROWAVE FIELD-EFFECT TRANSISTORS**

The objective of this work was to enhance the understanding of the operation of microwave field effect transistors (FET's), in order to guide materials choice and design to realize improved performance measured in terms of noise figure, frequency response or bandwidth, or power output. In order to achieve these objectives two-dimensional computer simulations of FETs were performed. Concepts developed here were applied to test transistor fabrication in order to verify the simulation results.

Work was also performed on the study and fabrication of Schottky barrier gate electrodes with relatively high barrier heights on small bandgap semiconductors, as might be needed for MESFETs fabricated of ternary and quaternary compounds.

In the two-dimensional transistor analyses the fields and charge density and velocity profiles are obtained from finite different solutions of Poisson's equation and the current flow equations, utilizing successive relaxation methods. Field-dependent velocities and isotropic diffusivities are used in these analyses. The simulations showed that an experimentally observed higher feedback capacitance in indium phosphide FET's, compared to GaAs devices, is due to reduced dipole layer formation in the gate-drain volume due to substrate conduction, not, to first order, to the shape of the indium phosphide velocity field curve. On the other hand, a large drain conductance in InP is due to a combination of unavoidable materials properties, such as large peak-to-valley ratio and large high field diffusivities, and the intrinsically low Schottky barrier height.

Insight was also obtained into the role of velocity overshoot in short channel FET's. While agreement between theoretical and experimental results for 1 micron gate GaAs, InP, and Si devices was very good, the experimental 1/2 micron gate compound semiconductor devices behaved, unexpectedly, better than predicted by the simulations. The

strong suggestion exists, then, that velocity overshoot, which could explain the discrepancy, plays a strong role in devices in the submicron scale range.

In larger devices, electron transit time through the channel was shown to depend more on the shape of the velocity-field characteristic than on the value of low-field mobility; thus, InP, which has a mobility about half that of GaAs but a much higher peak electron velocity which, significantly, extends over a wider range of fields than that in GaAs, should have considerably better high-frequency performance, for a certain range of gate lengths and drain voltages, than GaAs.

Circuit simulation results showed that GaAs MESFET's can switch about twice as much current as their Si counterparts for equal voltage swings. This difference is largely due to the larger low field mobility in GaAs, which results in lower parasitic resistances, and the larger diffusion coefficient in this material, which allows more charge to flow under the gate for a given gate voltage. However, due to the same factors, GaAs MESFET's had considerably higher gate capacitance than Si MESFET's. The direct cause of this higher capacitance is the more gradual depletion layer in the GaAs device. Other parasitic capacitances, however, were found to be similar in value.

MESFET inverters using buffered FET depletion mode logic were also analyzed. The GaAs inverter was shown to switch about 2-1/2 times faster than a similar inverter made with Si. The silicon inverter, however, dissipated about half as much power as the GaAs inverter.

Attempts to fabricate high performance Schottky barrier FET's in samples of GaInAs obtained from Bell Laboratories and Thomson-CSF led to a search for a means to modify the effective metal/Schottky barrier height by interfacial oxides. Such interfacial oxides have been utilized to reduce reverse leakage current density, and therefore increase apparent chottky barrier height, in Au/Si, Au/InP, and Au/GaAs systems. This search led to development of a method of obtaining quasi-Schottky barriers on compound semiconductors, such as GaInAsP, which have a small band gap and which, consequently, exhibit very small barrier heights unless special metal/semiconductor fabrication techniques are developed.

It was shown experimentally (and confirmed by a simple theoretical approach) that very thin ($<$ 100 Angstrom) interfacial oxide layers may be used to increase the effective barrier height of Au/InP and Au/GaInAs Schottky barriers. The results, which confirmed earlier studies on InP, extended the technique to GaInAs, and showed how it could be extended to GaInAsP, should be of great use in the fabrication of MESFET's made of these materials. In the experiments, barrier height on a specific sample of GaInAs was increased from about 0.2 eV to .49 eV through use of a 50 Angstrom oxide layer between metal and semiconductor. Breakdown voltages of oxides produced by various methods were also studied; chemically deposited (CVD) oxides were shown to be best of the various types available.

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Personnel

T. Wada - Masters Degree - January 1979
J. Faricelli - Masters Degree - January 1981
J. Nulman - 1979-1980
V. Morgan - 1978-1979

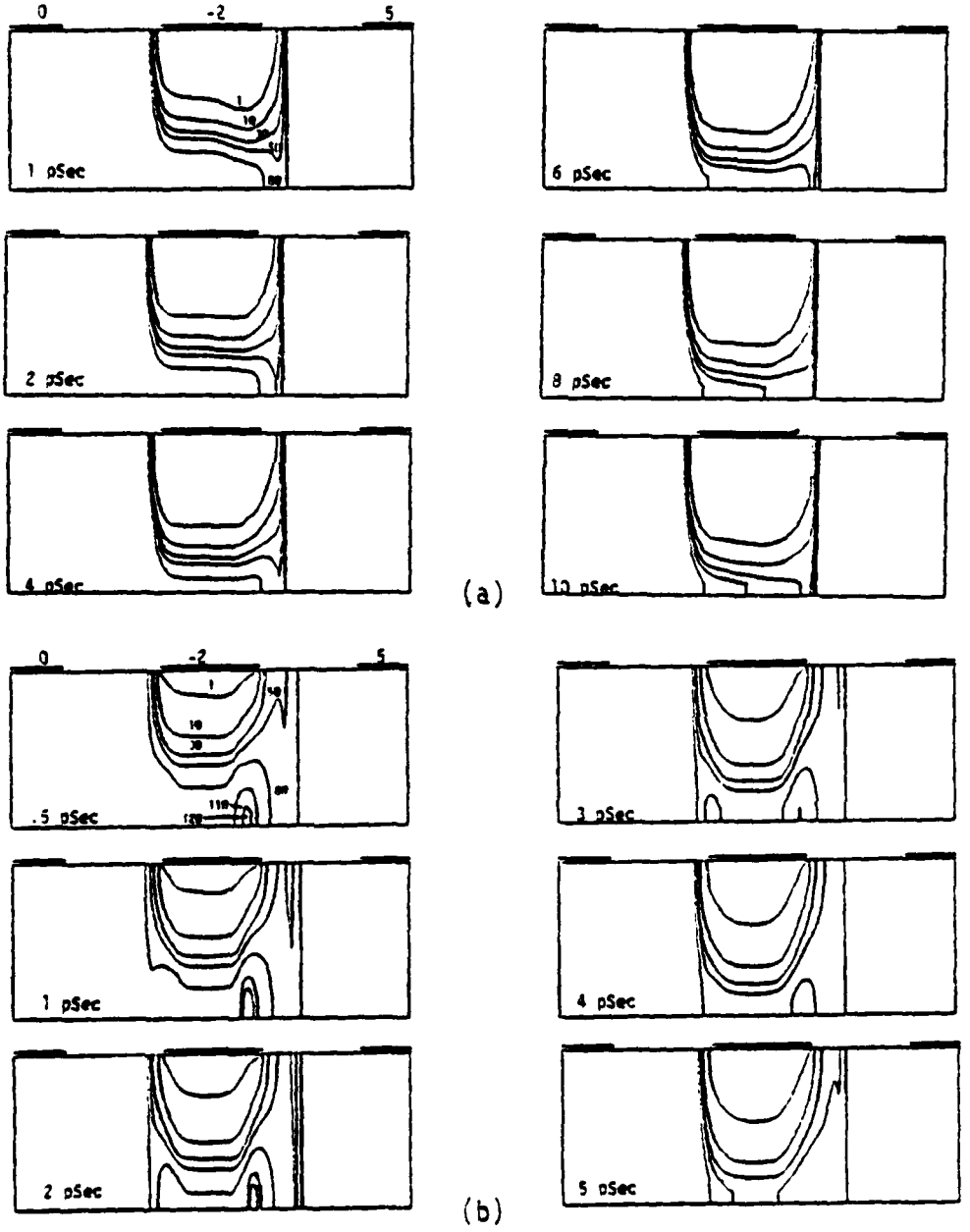
Technology Transfer

Technology and the results of analyses performed under this project heading are now in use in the following locations:

1. Technology for the production of quasi-SCHOTTKY-BARRIER GATES on COMPOUND SEMICONDUCTORS 9InP, GaInAsP, etc.) has been the subject of wide interest among experimenters in the field, as can be judged by the large number of requests for reprints received.

2. The results of TWO-DIMENSIONAL ANALYSIS OF SHORT-CHANNEL MESFET's have also excited wide interest. Some industries have begun work on short-channel Si MESFET's due partially to the results of these analyses; such industries include Texas Instruments, Tektronix, Burroughs, and Xerox Microelectronics. At least one microwave device laboratory (Varian Associates) has been reassessing its original conclusions on the basis of the conclusions obtained in this project section on the performance to be expected of InP devices.

The two-dimensional MESFET simulation program CUPID has been found to be useful in the following companies: Xerox Corporation, General Electric, Hewlett-Packard and Bell Telephone Laboratories.



Time sequence of mobile charge contours during gate pulse transient of 1μm gate MESFET. Contours are in percent of doping density ($10^{17}cm^{-3}$). a) Si MESFET, b) GaAs MESFET

W. H. KU

5/1/77 - 4/30/81

TITLE: **ADVANCED DESIGN TECHNIQUES FOR MICROWAVE GaAs FET AMPLIFIERS**

An integrated design approach for microwave GaAs FET amplifiers has been developed using analytical and computer-aided design (CAD) techniques. Significant contributions have been made toward the understanding of device-circuit interactions and derivations of explicit fundamental device-circuit limitations for state-of-the-art GaAs MESFETs. Computer-aided synthesis (CAS) techniques have been developed for both lumped and distributed matching networks for the design of broadband low-noise and high-power MESFET amplifiers.

Using the distributed synthesis program, matching networks are synthesized directly in distributed forms with arbitrarily prescribed gain slopes, bandwidth and impedance transformation ratio with exact tapered-magnitude maximally-flat and equiripple gain characteristics. To demonstrate and verify the computer-aided synthesis techniques, broadband GaAs MESFET amplifiers have been designed using 0.5 μm and 1.0 μm gate-length MESFETs. Experimental medium-power GaAs MESFET amplifiers covering 6-18 GHz have been designed and fabricated.

An optimum design theory for broadband low-noise GaAs MESFET amplifiers have also been developed. The design theory is based on a simplified noise equivalent circuit of the GaAs MESFET and analytical and CAD techniques for broadband FET amplifiers. The simplified noise model relate physically measurable device parameters to the device noise figure and optimum noise source impedance. It has been shown that the noise performance of a GaAs FET can be adequately described by two uncorrelated noise sources. The input noise source is the thermal noise generated in the various resistance in the gate-source loop. This noise source is frequency dependent and it can be calculated from the equivalent circuit of the FET. The output noise source is frequency independent but is a function of drain current and voltage.

This simplified noise model has been completely developed and has been verified experimentally by actual noise measurements of a large number of state-of-the-art 1 μm and 0.5 μm gate-length GaAs MESFETs. It

has also been shown that this simplified noise model can be applied directly to the optimum design of low-noise FET amplifiers. Based on the model, the minimum noise figure and the optimum source impedance over the specified frequency band can be calculated. The input matching network is first designed to provide the optimum noise match and the output matching network is then synthesized to provide a flat amplifier gain. For a typical 0.5 μm gate-length FET with an assumed noise figure of 2 dB at 10 GHz and using the simplified noise model, it is predicted that an input matching network with an approximate 4 dB/octave taper will provide an optimum noise match. Using this result, a 6-18 GHz MESFET amplifier can be designed to provide a flat noise figure of 3.2 dB ± 0.3 dB across the entire frequency band.

In the design of monolithic microwave integrated circuits (MMICs), the matching networks consist of lumped reactive elements and/or transmission-line elements. Lumped elements are often essential since they occupy less GaAs chip area and have broader bandwidth capability. Furthermore, in MMICs, the lumped elements realized as matching circuit components will be lossy. Existing design techniques are restricted to lossless matching networks. A major achievement in our research is the successful development of an exact synthesis procedure for lossy matching networks which are essential for the design of MMICs. The lossy synthesis problem we have solved is for the general case of unequal inductor and capacitor losses with arbitrary circuit topology and realizable gain functions. In addition, we have studied the design of coupled coils and mixed lumped-distributed matching networks for monolithic realizations of broadband GaAs MESFET amplifiers.

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7. "Synthesis of Interstage Matching Networks", W. H. Ku (Invited Paper) Modern Microwave Circuit Design: Theory and Practice Short Course on GaAs FET Theory and Applications, IEEE Microwave Theory and Techniques Group, San Francisco Chapter, Stanford SLAC, Palo Alto, CA (Jan. 22, 1977).

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10. "Synthesis of Distributed Networks and Their Applications to the Design of Microwave Solid-State Amplifiers", W. H. Ku (Invited Paper) 1979 Int. Symp. on Circuits and Systems, Tokyo, Japan (July 17-19, 1979).

11. "Computer-Aided Design (CAD) of Microwave GaAs MESFET Amplifiers", W. H. Ku and W. C. Petersen, Proc. Seventh Biennial Cornell Conf. on Active Microwave Semiconductor Devices and Circuits, Ithaca, NY, p. 275 (August 14-16, 1979).

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15. "Modelling of Dual-Gate MESFETs With Second Gate Forward Biased", P. C. Chao and W. H. Ku, Electronics Lett., Vol. 17, No. 16, p. 574-576 (August 1981).

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Personnel

Masters Degree

C. Scott - August 1981

Ph.D. Degree

L. Liu - May 1981

H. J. CARLIN

3/1/70 - 4/30/81

TITLE: **WIDE BAND CIRCUITS AND SYSTEMS**

Introduction

The major task we have set ourselves under this program is to develop a new method of broad band circuit design which optimizes the transfer of available power from a resistive generator source to a complex load. We have also considered the complex generator - complex load problem.

The classic analytic theory which applies to the resistive source problem suffers from several major defects.

1. It demands the complex load be modeled by an equivalent circuit based on experimental data.
2. It requires the formulation of an analytic transfer function class with appropriate properties in the complex frequency plane and which is compatible with the modeled complex load, the physical requirements of the equalizers, and the gain shape, and bandwidth specifications. This is extremely difficult for other than simple loads and modest specifications.
3. It presumes that the chosen transfer function class can have its parameters adjucted to produce a true optimum e.g., maximum pass band gain (maxi-min) consistent with equalizer complexity.

Brief Summary of Research Results

A. Resistive Generator - Complex Load

This portion of the research program was concerned with developing a new Computer Aided Design (CAD) technique which by-passes the procedures of analytic gain bandwidth theory and only processes real frequency data i.e., there is no direct recourse to the complex frequency plane. Our research has resulted in a new CAD technique which from a practical design point of view seems superior in most major respects to the classic analytic procedures. The new method is termed the "Real Frequency Technique."

1. The method does not require modeling of the complex load by a circuit. The measured data are processed directly. For example, regarding a microwave FET amplifier device as a 2-port with measured scattering parameters given, input and output equalizers have been designed directly. In the process it is not even necessary to assume that the FET is unilateral. Such design equalized for gain and/or noise figure are given in Ref. 1, 2, 3, and 4.
2. As a result of the new method we have been able to show that designs via the "Real Frequency Technique" are obtainable for cases where the difficulties of applying the classic analytic approach are so formidable that the latter procedure is virtually inapplicable. The method has also been used to good advantage in the nonlinear problem of a wide band tuning circuit for a varactor tuned oscillator. Ref. 5.
3. Perhaps most surprising of all is the fact that even in cases where the analytic theory is applicable the "Real Frequency Method" yields superior results. Thus we have made a comparative study of the new "Real Frequency" method vis a vis the analytic theory in cases where the analytic solution can be worked out. We have determined broad band equalizer designs for given complex loads via the analytic theory using Chebychev equal ripple transfer functions. The same loads have then been equalized using the "Real Frequency Method." The Real Frequency designs have been superior in the following respects:
    1. Gain-bandwidth performance. The Real Frequency designs have larger values of "maxi-min" pass band gain.
    2. Pass band tolerance. The Real Frequency designs generally show less fluctuation between maximum and minimum pass band gain. In effect they possess superior pass-band flatness.
    3. Equalizer Complexity. The Real Frequency equalizers have the same or fewer elements than those designed from Chebychev transfer functions.

Also in many cases the analytic method requires coupled coil or transformer sections. The superior performance specifications of the "Real Frequency Design" equalizers under comparison are all accomplished without transformers. Reference 5 presents an analysis of these results and gives numerous examples. Some of these are summarized here in Tables *I* and *II*.

B. Complex Generator - Complex Load

In problems such as amplifier interstage design, an equalizer must optimally transfer a signal from a complex generator impedance to a complex load. The analytic theory is still not complete for this case, but such as it is the difficulties of application are even more severe than in the case of a resistive generator.

The Ph.D. research of Mr. S. Yarman is involved with the extension of the CAD "Real Frequency Method" to the complex generator - complex load case; the "Double Matching Problem." We have some preliminary results which indicate that the "Real Frequency Method" can be extended to the "Double Matching Problem" and furthermore again indicate superior equalizer designs. Some initial comparative results are presented in Table 3.

C. Matching of a Prescribed 2-port

As a variant of the "double matching" problem, Prof. Y. S. Wu has been considering the case of a prescribed two-port which is to be equalized at both input and output simultaneously without making any assumptions on the unilateral nature of the given 2-port. Prof. Wu is a Visiting Professor from the University of Tsientsin, People's Republic of China. He has formulated a CAD method of design which generalizes the procedure of Ref. 5 by proceding directly to an optimization of the parameters of the two equalizers without the necessity of iterating each successively. We are now applying the method to specific amplifier designs (for optimum gain and noise figure) to evaluate the efficiency and ease of applicability of the new algorithm.

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4.* H. J. Carlin and J. J. Komiak, "A New Method of Broadband Equalization Applied to Microwave Amplifiers", IEEE Trans. on Microwave Theory and Techniques, Vol. MTT-27, No. 2, February 1979, pp. 93-99.
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*Published under contract.

PERSONNEL

H. J. Carlin	Professor of Electrical Engineering
J. J. Komiak	Graduate Research Assistant. Received Ph.D. under the contract June 1978.
S. Yener	Graduate Research Assistant. Will receive Ph.D. December 1981.
Y. S. Wu	Visiting Professor, Tsientsin University (No charge to contract).

TRANSFER OF INFORMATION

H. J. Carlin gave a series of invited seminars related to the present research program at the following places:

1. Carniegie Mellon University - July 10, 1978.
2. Case-Western Reserve University - October 5, 1978.
3. University of Pennsylvania - October 27, 1978.
4. National Center for Telecommunications - Paris, France - October 1979.
5. University College, London - December 1979.
6. Technion University - Haifa, Israel - March 1979.

7. University of Turin - Turin, Italy - April 1979.
8. University of Limoges - Limoges, France - May 1979.

TABLE I: COMPARISON OF EQUAL RIPPLE and REAL FREQUENCY EQUALIZERS

LCR LOADS, LOW PASS DESIGN

Pass-band $0 \leq \omega \leq 1$

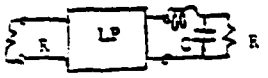
CASE 	DESIGN	G_0 (c)	Δ (d)	No. of Equalizer Elements	No. of Transformers
L = 1.3, C = 1.2, (a) R = 1	Equal Ripple (e) n = 3	0.772	0.120	3	1
As above (a)	Equal Ripple n = 4	0.831	0.063	4	1
As above (a)	Real Freq.	0.849	0.045	3	0
L = .55, C = 5, (b) R = 1	Equal Ripple n = 5	0.441	1.136	3	0
As above (b)	Equal Ripple n = 4	0.582	0.200	4	1
As above (b)	Real Freq.	(a) 0.601 (b) 0.646	(a) 0.259 (b) 0.168	(a) 3 (b) 4	(a) 0 (b) 0

TABLE II: EQUAL RIPPLE vs. REAL FREQUENCY EQUALIZERS, BANDPASS CASE

Load: L = 0.55, C = 5.0, R = 1. Pass-band: $0.2 \leq \omega \leq 1.0$

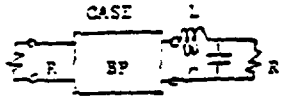
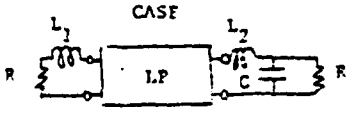
CASE 	G_0 = Max-Min Pass-band Gain	Δ = Pass-band Gain Variation	Total Equalizer Elements	No. of Transformers
Real Frequency	0.525	0.238	3	0
Real Frequency	0.628	0.081	5	0
Chebyshev	0.522	0.185	10	1
Chebyshev	0.587	0.090	14	1

TABLE III: DOUBLE MATCHING, EQUAL RIPPLE vs. REAL FREQUENCY EQUALIZER

Load: $L_1 = 1$, $L_2 = 2$, C = 1, R = 1. Pass-band $0 \leq \omega \leq 1$

CASE 	G_0	Δ	No. of Equalizer Elements	No. of Transformers
Real Frequency	0.932	0.046	3	0
Equal Ripple	0.847	0.181	3	1

NOTES

(a) Ideal flat maximum gain level 0.92.

(b) Ideal flat maximum gain level 0.715

(c) G_0 is maximum value of minimum pass-band gain

(d) Δ = Pass-band gain variation, i.e. $(G_{MAX}/G_0) - 1$. In all cases Δ is value corresponding to optimum G_0. For Chebyshev $\alpha = 0^\circ$.

(e) Gain = $\frac{2}{1 + \omega^2 + \omega^4}$

C. L. TANG

5/1/80 - 4/30/81

TITLE: **DYNAMIC AND SPECTRAL CHARACTERISTICS OF SEMICONDUCTOR LASER MATERIALS AND STRUCTURES**

INTRODUCTION

The objectives are to gain a thorough understanding of and to develop the means to control the dynamic and spectral characteristics of semiconductor laser structures and materials. Joint Services Electronics Program support for this project started in December, 1980. The project was initially supported by other grants and contracts and has been supported jointly by these grants and contracts and JSEP since December, 1980.

PROGRESS

1. Injected Carrier Induced Refractive-Index Change in Semiconductor Lasers[1]

A red-shift in the diode modes with increasing optical feedback is observed in external-cavity $Al_xGa_{1-x}As$ injection lasers. This shift is due to a change in the refractive index in the active region resulting from a reduction in the population-inversion induced by the optical feedback. This leads to a new determination of the carrier dependence of the refractive index at the laser wavelength in the active region of semiconductor lasers independent of current induced thermal effects. The contribution to the refractive index due to the injected carriers in the active region of semiconductor lasers plays a key role in a number of important characteristics of GaAs lasers.

2. Coherent Optical Interference Effects in External-Cavity Semiconductor Lasers[2]

A broadening of the apparent linewidth of the semiconductor laser modes with external-feedback is observed. This is shown to be due to the coherent nature of the feedback and multiple reflections in the external-cavity semiconductor laser taking into account such coherent optical effects is developed. The inclusion of these effects is also shown to be important in the interpretation of the threshold data of such lasers.

3. Active Mode-Locking of Linear and Ring External-Cavity Semiconductor Lasers[3]

Pulses on the order of 6 to 8 pico-seconds are obtained in an actively mode-locked external-cavity anti-reflection coated semiconductor laser. We also report the mode-locking of a ring-cavity semiconductor laser.

4. Radiative and Non-radiative Lifetimes in the Active Region of Semiconductor Lasers at High Injection Levels

The spontaneous and non-radiative lifetimes of the injected carriers play an important role in determining the static and dynamic behavior of semiconductor lasers. A systematic experimental and theoretical study of these lifetimes has been carried out at high injection levels where bimolecular recombination is important. At these high injection levels the decay process does not follow a simple single exponential decay and the general behavior is quite complicated. By using a nonlinear optical up-conversion process, the time dependence of the decay has been measured with a resolution of approximately 0.1 nsec which corresponds to the pulse width of the mode-locked Ar-laser pump pulse. A detailed theory and numerical computation have been carried out. The results show that the non-exponential decay can be accounted for by including both bimolecular recombination and partial amplification of the observed spontaneous emission from the laser structure.

5. Metalorganic Chemical Vapor Deposition

This is a joint project with several other groups. Our interest is in using the system to grow laser structures and materials suitable for optical applications. The project is well under way and we expect the system to be completed during the next funding period.

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3. "Active Mode-Locking of Linear and Ring External-Cavity Semiconductor Lasers", A. Olsson and C. L. Tang, J. Quant. Elect. (scheduled for Oct. 15, 1981).

Personnel

The following persons received full or partial support from JSEP during the reporting period:

A. Olsson
A. Schremer
V. Kreismanis

J.M. BALLANTYNE AND D.K. WAGNER

5/1/80 - 4/30/81

TITLE: **HIGH SPEED RECEIVERS FOR OPTICAL COMMUNICATIONS**

The objectives of this task over a three-year period are to:

1. Construct a large area OPFET which is compatible with optical fibers.
2. Monolithically integrate the OPFET and LAEPOD detectors with low-noise, high-speed preamplifiers.
3. Develop MOCVD growth technology to provide materials suitable for monolithic optical receivers.

This task was a new one added in the 1980-81 year and hence the progress reported here is for the first year of that task.

Progress on all three objectives was made this year. S. Wojtczuk constructed large area OPFET detectors in an interdigitated, notched design. He also constructed interdigitated and single OPFET detectors monolithically integrated with a three stage, six active device amplifier. Tests are in progress on both the devices and the amplifier. To date, low frequency gains are 14 and a remarkably uniform spatial response has been measured on the interdigitated, notched OPFET. Tests on noise and speed of the integrated receiver are in progress, and gain-bandwidth products of over 250 GHz are expected. Preliminary results of this work were reported in Ref. 20.

Dr. R. Griffiths, Dr. D. K. Wagner, students - V. Kreismanis and R. Shealey, and technician - Mr. Chuck Harding have constructed our MOCVD growth system during the year. This system is nearly complete and is now being installed in its permanent room on the 4th floor of Phillips Hall. Growth in the system should begin within a few weeks.

Personnel

J. M. Ballantyne - Professor

D.K. Wagner - Sr. Research Associate

H. Beneking - Visiting Professor

R. Griffiths - Visiting Research Associate

S. Fischer, B. Kushner, A. von Lehmen and S. Wojtczuk - Graduate Research Assistants

Publications and information transfers are indicated in the following list of publications for J. Ballantyne and members of his group during the 1980-81 year.

Publications

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2. "Short Transit Time Photoconductive Detectors for High Speed Optical Communications", J.C. Gammel, G.M. Metze, H. Ohno, J.M. Ballantyne, paper IIIB-5, 38th Annual Device Research Conf., June (1980), Ithaca, NY.
3. "Characterization of Grain Boundaries in GaAs by Scanned Photoluminescence and Diffusion Length Measurements", R. Fletcher, D.K. Wagner, and J.M. Ballantyne, paper P-3, Tech. Program Electronic Materials Conference, p. 49, June (1980), Ithaca, NY. Published by The Metallurgical Society of AIME. (Abstract only).
4. "Optical Methods for Characterizing GaAs for Polycrystalline Solar Cells and Photoconductive Detectors", J.M. Ballantyne. Invited talk, Xerox Webster Research Labs, Webster, NY, 16 July 1980.
5. "High Resolution Optical Methods for Characterization of Polycrystalline GaAs Thin Films", D.K. Wagner, R.M. Fletcher and J.M. Ballantyne, IEEE Trans. Electron Devices, ED-27, 2213 (1980).
6. "A Photoconductive Detector for High Speed Fiber Communication", J.C. Gammel, G.M. Metze, and J.M. Ballantyne, IEEE Trans. Electron Devices, ED-28, 841 (1981).
7. "High Speed Photoconductive Detectors Using GaInAs", J.C. Gammel, H. Ohno, and J.M. Ballantyne, IEEE J. Quantum Electronics, QE-17, 269 (1981).
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9. "Optical Techniques for Characterizing III-V Compounds for Applications in Photoconductive Detectors and Solar Cells", J.M. Ballantyne. Invited seminar, Xerox Webster Research Center, July 16, 1980.

10. "Double Heterostructure $Ga_{0.47}In_{0.53}As$ Integrated Photoreceiver", J. Barnard, C.E.C. Wood, L.F. Eastman, and J. Ballantyne, IOOOC'81 Conf., San Francisco, CA, April (1981).

11. "The National Research and Resource Facility for Submicron Structures", J.M. Ballantyne and E.D. Wolf, 1981 Southcon Professional Program, Session 3 Microstructure Engineering for Microelectronics, pp. 1-9 (1981). Published by Electronic Conventions, Inc., 999 N. Sepulveda Blvd., El Segundo, CA 90245.

12. "Gallium Arsenide Materials for Applications in Solar Energy Conversion and Optical Communications", J.M. Ballantyne Seminar. Eastman Kodak Research Labs, Rochester, NY, 26 January 1981.

13. "U.V. Grating Polarizers", G.J. Sonek, D.K. Wagner, and J. Ballantyne, post deadline paper at the Sixteenth Symposium on Electron, Ion and Photon Beam Technology, May (1981), Dallas, TX. Submitted for publication.

14. "Microfabrication Techniques", J.M. Ballantyne; invited lecture at International Symposium on Telecommunications, Kuwat, April (1981), sponsored by Kuwait Foundation for Advancement of Science, proceedings published by Academic Press.

15. "Device Research in the National Submicron Facility", J.M. Ballantyne, invited seminar at the Department of Electrical Engineering, The Technion, Haifa, Israel, April 12, 1981.

16. "Research Programs in the National Submicron Facility at Cornell", J.M. Ballantyne, Seminar at the Department of Applied Physics, Hebrew University, Jerusalem, Israel, April 14, 1981.

17. "Homostructure Planar-Doped-Barrier Diode as an Optical Detector", A. von Lehmen and J.M. Ballantyne, postdeadline paper at the Joint Meet. of the NSF Grantee-User Group on Optical Communications and the Department of Commerce Optical Communications Task Force, May 27-29, (1981), Washington Univ., St. Louis, MO, to be published.

18. "Photoconductive and Planar-Doped-Barrier Optical Detectors in III-V Compounds", J.M. Ballantyne, invited talk, U.S.-Frnce Workshop on GaAs Microstructures and High Performance Devices, Boston, MA, June 8-10 (1981).
19. "Microfabrication Techniques for Devices", J.M. Ballantyne, invited seminar, Comsat Laboratories, 9 July, 1981.
20. "Monolithically Integrated Active Optical Devices", J. Ballantyne, D.K. Wagner, B. Kushner and S. Wojtczuk. Conference on Optical Information Processing for Aerospace Applications, Aug. (1981), NASA LaRc-OAST (Proceedings to be published).

P. R. McISAAC

5/1/77-4/30/79

TITLE: **DEVELOPMENT OF SYMMETRY ANALYSIS METHODS FOR PERIODIC STRUCTURES**

The general focus of this task for its two year duration (1977-79) was the development of symmetry analysis methods for periodic structures for microwave, millimeter, and optical applications. The class of waveguide structures explored were those which are periodic along the waveguide axis; the media involved can be inhomogeneous and anisotropic. The study included periodic waveguides containing directed media; that is, active or passive media whose ac susceptibilities may depend on a dc magnetic field and/or the dc drift velocity of charge carriers. The general modal properties of periodic waveguides were investigated and the influence of the structure symmetry explored. A summary of the results is given here.

The stem groups, a subset of the complete set of space groups, are the appropriate set of symmetry groups applicable to periodic waveguides. The stem groups were enumerated for structures with either simple or directed media.

The symmetry properties of a structure determine the general modal properties. All structures belonging to the same stem group have similar modal properties. The modal properties include the number of mode classes, the degeneracies between mode classes, and the electromagnetic field symmetry characteristic of each mode class. In the case of structures with directed media, it was found that the complete mode spectrum must include the modes of the original waveguide together with the modes of the complementary waveguide. The complementary waveguide is obtained by reversing the direction of the dc magnetic field and the dc drift velocity of the charge carriers. Depending on the circumstances, degeneracy between mode classes may occur between mode classes of the original waveguide, or between a mode class of the original waveguide and a mode class of the complementary waveguide. Identification of the stem group of a structure enables one to predict the general mode properties without having to solve a

boundary value problem.

The bidirectionality of periodiç waveguides was studied. A waveguide is termed bidirectional if each mode with a propagation constant $\gamma(\omega)$ can be matched with a mode whose propagation constant is $-\gamma(\omega)$. Many common waveguides are bidiretional with each mode yielding both the propagation constants $+\gamma(\omega)$ and $-\gamma(\omega)$. Some waveguides; for example, a helix, are bidirectional with $+\gamma(\omega)$ and $-\gamma(\omega)$ associated with separate, and distinct, modes. It was found that the occurrence of bidirectionality depends solely on the symmetry of the structure. That is, those structures whose stem group includes symmetry operations which reverse the waveguide axis aare bidirectional. In particular, reciprocity is neither a necessary, nor a sufficient, condition for bidirectionality.

A general reciprocity theorem applicable to all causal and linear media was derived from the Onsager relations. The physical basis for the general reciprocity theorem is the time-reversal invariance of the microscopic equations of motion for linear media. Based on this theorem, the general mode orthogonality relations for periodic waveguides were derived. This was apparently the first derivation of the mode orthogonality relations for periodic waveguides containing directed media. These results were published in the paper: "A General Reciprocity Theorem", IEEE Trans. Microwave Theory and Techniques, vol. MTT-27, pp. 340-342, April 1979.

C.A. LEE

5/1/77 - 4/30/79

TITLE: **CARRIER MULTIPLICATION MEASUREMENTS IN SEMICONDUCTORS**

Introduction

In addition to early studies of silicon and GaAs carrier multiplication, germanium p-n junctions have now been fabricated and multiplication measurements have been made on them.

Progress

We started with p-type Ge wafers of resistivity of approximately 0.5 Ωcm, cleaved in the <111> plane. The wafers were chemically polished using a 2:1 solution of clorox and water, and then thinned down to about a 5-7 mil thickness, using a $HF-HNO_3$ etch. Arsenic was then diffused into the wafer by a vacuum diffusion process, at about 800°C, for about 45 minutes, thus ensuring a fairly deep (≃ 2 mils) junction. On one side of this wafer (with As diffused into it), successive sputtering of chromium (≃ 500 Å thick) and gold (≃ 500 Å thick) was done. This side of the wafer was then masked and the wafer thinned down to ≃3 mils, by using the same acid etch as above. This also removed the n layer from the etched side. This 3 mil thick wafer was then scribed, using a diamond scriber, into diodes of 10 mils square. These diodes were then bonded to a 20 mil wide gold ribbon and etched down to about 7-8 mils square. They were then ready for making multiplication measurements.

The diodes thus made were found to have a breakdown voltage of approximately 20V. First of all, the capacitance of the diode as a function of the applied reverse bias, was measured.

The multiplication measurements were made on the diode using each of the following light sources to generate the carriers for the multiplication:

i) Tungsten lamp

ii) Mercury-vapor lamp.

Measurements were also made using each of the above sources, with a 620 nm filter to select a narrow wavelength for the source,

in order to obtain multiplication generated by a majority of one kind of carrier.

Multiplication measurements were made to determine, first, the multiplication generated by electrons only, and then multiplication generated by holes only, i.e., both Mn and Mp, in the same diode. An arrangement was made by means of which the diode could be irradiated from either the n or p-side. These measurements are as shown in Figures 1 and 2.

Using the values of α and β for Ge, as obtained by Miller,[1] and others,[2] a theoretical calculation of Mn and Mp was performed. The close agreement obtained between the theoretical and experimental values of α and β seem to corroborate Miller's values for α and β.

Measurements of the intrinsic avalanche response time and comparison with theory have been completed erlier for silicon, and now for GaAs including the crystal orientation dependence,[3,4] and germanium.[5]

Personnel Associated with this Task

1. Charles A. Lee - Principal Investigator
2. Sucharita Basu - Graduate Student (M.S. degree Jan. 1979)

References

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2. D.R. Decker and C.N. Dunn, "Determination of Germanium Ionization Coefficients from Small Signal IMPATT diode Characteristics", IEEE Trans. on Elec. Dev., Vol. ED-17, No. 4, pp. 290-299, April 1970.
3. C.A. Lee, J. Berenz and G.C. Dalman, "Determination of GaAs Intrinsic Avalanche Response Time from Noise Measurements", Proceedings of the Sixth Biennial Cornell Conference on Active Microwave Semiconductor Devices and Circuits, Ithaca, NY, pp. 233-245, August 1977.
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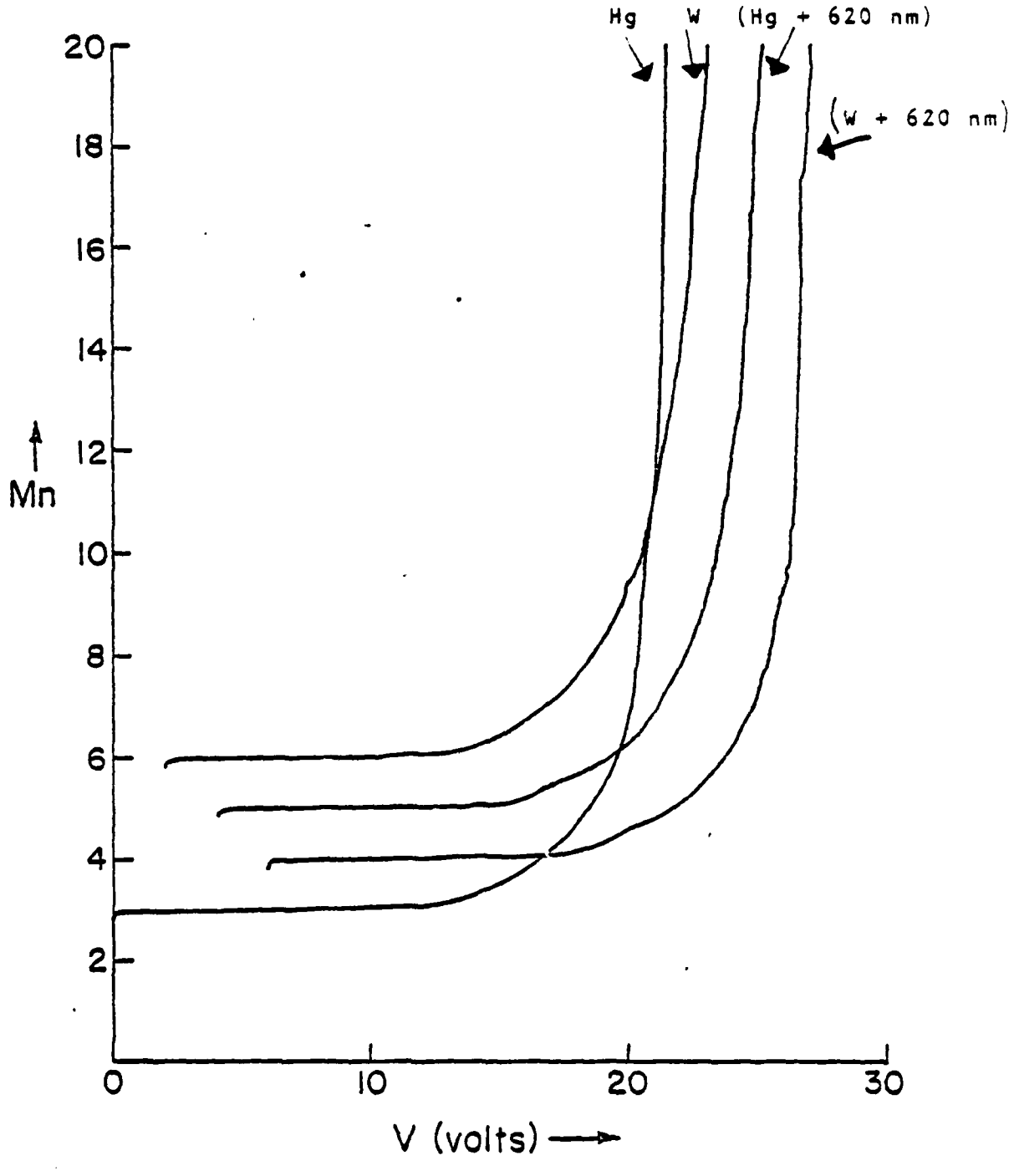

Figure 1. Multiplication Measurement for Mn Diode with p-side up.

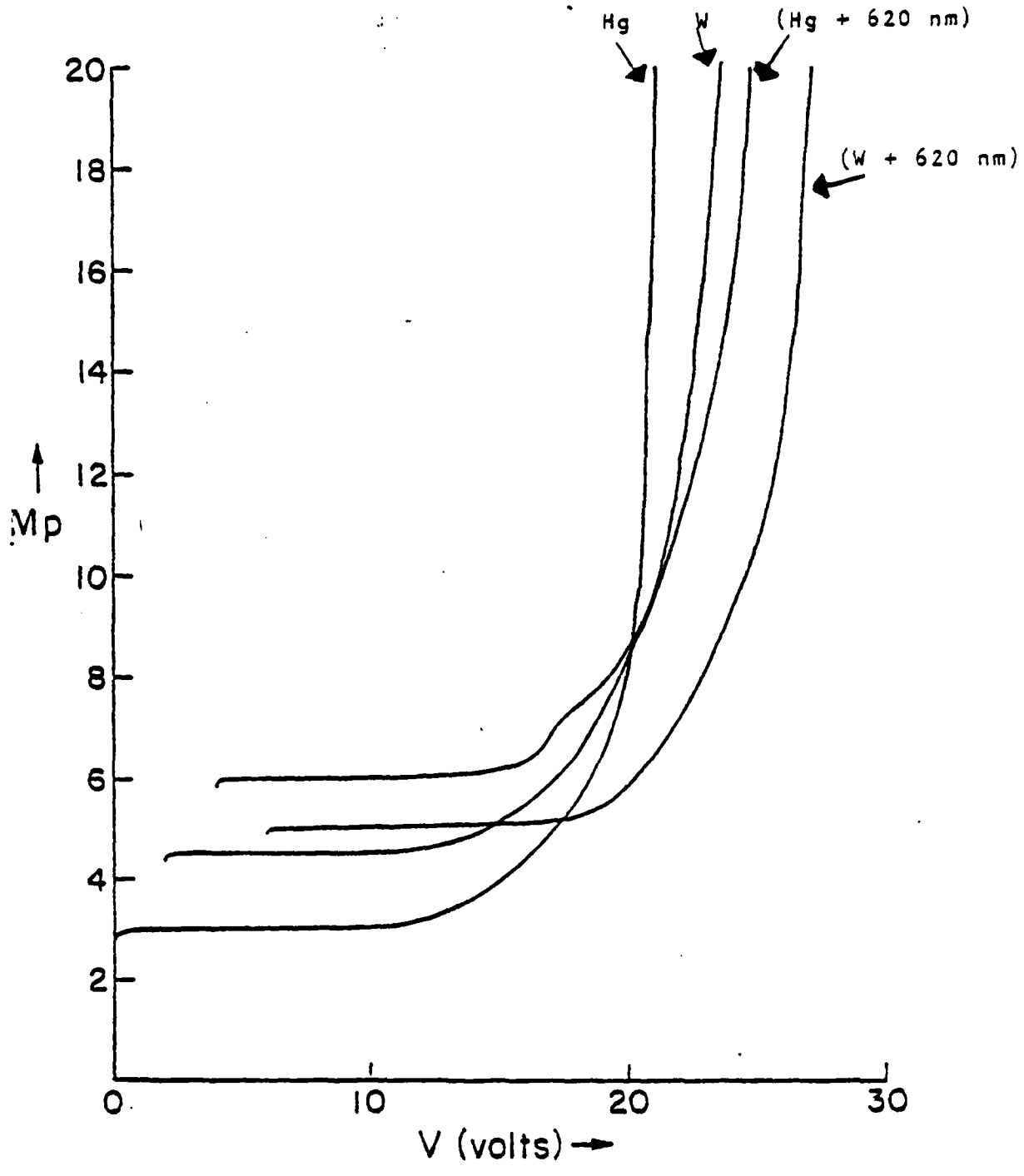

Figure 2. Multiplication Measurements for Mp Diode with n-side up.

5. S. Basu and C.A. Lee, "Compatibility of Ionization Rates and Intrinsic Response Time in Ge Junctions".

Transfer of Technology

Raytheon Corporation: D.H. Statz, Dr. R. Bierig and Dr. R. Pucell have been the people with which most extensive contact has been made. There is and has been a continuous interaction concerning the evaluation of diodes and material.

Varian Associates, Inc.: Principle contacts have been Dr. J. Berenz, Dr. T. Hierl, and Dr. Berin Fank. Measurements of orientation dependence of intrinsic response time in GaAs and response time measurements of InP have been carried out jointly.

SAMSO: Presented 4/26/79 (with G.C. Dalman) Major Chandler Kermedy successful results on a one diode eleven watt linear Impatt amplifier with 3 order intermodulation distortion of less than -15 dB below two tone carrier power.

Wright Patterson Avionics Lab: Presented 6/4/79 (with G.C. Dalman) to Dr. R. Kimmerly and Dr. R. Remski, linear amplifier results with constant voltage bias.

C.A. LEE and G.C. DALMAN

5/1/77 - 4/30/79

TITLE: **STUDY OF ION IMPLANTED SILICON COMPLEMENTARY N+PπP+ READ DIODES**

Introduction

The work reported here involves the study of $n^+p\pi p^+$ silicon Read IMPATT diodes. The first part of this report deals briefly with the reasons for undertaking a study of this particular structure. The second part summarized the main findings. Further details can be found in the Ph.D. thesis of A. Gupta.[1]

Motivation

Although the flat profile IMPATT is relatively easy to fabricate, it is limited in efficiency. The theoretical limit is approximately 12%, practical diodes reach about 10%. W.T. Read[2] was the first one to realize that a non uniform doping in the diodes space charge region that results in a narrow avalanche region and a relatively low electric field in the drift region greatly enhances the efficiency of the device. Misawa[3] tested $p^+n\nu n^+$ and metal $-n\nu n^+$ silicon diodes which were close approximations to the structure proposed by Read. The highest efficiency reported on these diodes was 11%. Misawa's experiment was repeated by R. Kwor[4] at Cornell University. He fabricated $p^+n\nu n^+$ silicon diodes by ion implantation and carefully studied the factors limiting the performance of these devices. He discovered that an avalanche phase delay ξ, of much less than 90^o was responsible for their poorer-than-expected performance. The reasons for a small phase delay are:

i) high reverse saturation current resulting in multiplications M, of less than 100 at the operating point.

ii) the saturation current exciting the avalanche is due to electrons from the heavily doped p^+ region even though most of the space charge is in the lightly doped n region. This is because of the stresses introduced in the p^+ region during numerous processing steps. This region is very heavily doped,

it has residual implantation damage, it has refractory metal metallization on one side and is thermocompression bonded to the diode package. All these factors produce a saturation current several orders of magnitude greater than that expected from the drift region.

Thus, the intrinsic response time of the avalanche region of these diodes is that corresponding to electron excitation ($\tau_l = \tau_{ln}$). In addition, the avalanche width of these diodes is $< .5$ μm. Therefore, τ_{ln} for this structure $< .4 \times 10^{-12}$sec.

With $M < 100$ and $\tau_l < .4 \times 10^{-12}$sec., $\omega M \tau_l \simeq 1.0$ at the design frequency of ≃8 GHz. Since $\tan |\xi| = \omega M \tau_l \xi$, this implies that the phase delay in these devices will be quite poor.

The intrinsic response time of a $n^+p\pi p^+$ Read diode will be approximately equal to τ_{lp} because holes from the n^+ region will constitute the majority of the saturation current. In silicon Read diodes τ_{lp} is about a factor 5 greater than τ_{ln} because in silicon the electron ionization rate is much greater than the hole ionization rate. Therefore, with an avalanche region of ≃.5 μm the response time of these diodes should be $\simeq 1.5 \times 10^{-12}$sec. This is a threefold improvement over the response time of the n-Read diodes. If, in addition, saturation currents can be kept low, this diode should have a significantly improved phase delay. The study of $n^+p\pi p^+$ Read diodes was undertaken for these reasons. The diodes were fabricated by implanting phosphorous and boron in πp^+ epitaxial silicon. It is usual practice to predamage the wafer surface in order to minimize channeling and obtain hyper abrupt doping profiles. It was decided not to predamage the wafer used to fabricate the p-diodes because previous experience has shown that the damage produced by this process is very difficult to anneal out completely. In addition, annealing temperatures of ≃1025°C were employed to ensure that the damage is removed as much as posible and the saturation currents are minimized.

Results

1) The p diodes ($n^+p\pi p^+$) showed an improvement in $\omega M \tau_l$ by a factor of approximately 3.6 over the n Read diodes ($p^+n\nu n^+$). Since τ_l for the p diodes is greater than that of the n diodes

by just about this factor, it appears that the saturation current density of the two diode structures is about the same in spite of the extra precautions taken in fabricating the p diodes. This, most probably, indicates a limitation of the ion implantation technique. It is well known that a complex network of defects is present in implanted layers even after they have been annealed at temperatures in excess of 1000°C. These defects could easily increase the saturation current by order of magnitude.

ii) The improvement in performance that should have been seen due to a higher avalanche phase delay was more than offset by an unusually large increase in the value of a_2, the curvature of the $(1/M\tau_1)$ function near the bia point. a_2 governs the rate at which negative conductance falls off as a function of increasing RF voltage. To be able to operate the diode at high power levels, it is necessary to have a_2 positive and as small as possible. Otherwise, the negative conductance at large signals is very poor.

Large signal measurements on the p diodes gave $a_2/a_0 = 4.5 \times 10^{-8}$ where $a_0 = 1/M\tau_1$ at the operating bias point. From small signal measurements under the same bias conditions, $M\tau_1$ was found to be equal to 4.47×10^{-11}sec. Thus $a_2 = +1008$ and $2\tau_t\xi_c^2 a_2 = 3.66 \times 10^4$, an extremely large value. In this expression τ_t is the transit time across the drift region and ξ_c is the DC breakdown field. This extremely large value of a_2 leads to a very poor performance at large signals even though the small signal negative conductance is of comparable value to other diodes of the same area.

This research has shown that some improvement in the avalanche phase delay can be obtained by exciting the avalanche by holes instead of electrons. However, substantial improvements can only be achieved if ways of reducing the saturation current density can be found. This might involve an extensive study of the metallization systems commonly used and their effect on the saturation current. It might also be more appropriate to diffuse the shallow n^+ region instead of implanting it in the interest of reduced radiation damage. The role played by a_2 is affecting large signal operation

is dramatically illustrated by the diodes fabricated in this study. It will be necessary to study other diode structures to get a better understanding of the parameters which control it.

In previous work, ion-implanted Si $p^+n\nu n^+$ Read structures had been fabricated and evaluated.[4] This work showed that the moderate efficiency obtained (9%) ws due to a very small intrinsic response time which gave rise to an avalanche phase delay of 35°-50° rather than the expected 85°-90°. These diodes had material parameters which were quite similar to those made in several industrial laboratories which had similar moderate efficiencies.

From this analysis of the $p^+n\nu n^+$ structure the short intrinsic response time ($\sim$ .3 ps.) implied that electrons comprised the major component of the saturation current. It was conjectured that in the complementary $n^+p\pi p^+$ diode holes would dominate the saturtion current and thus the governing intrinsic response time would be that characteristics of holes, τ_{lp}. Ion-implanted $n^+p\,\pi p^+$ were fabricated and tested.[5] It was verified that the intrinsic response time was a factor of three times larger than the $p^+n\nu n^+$ structure and the avalanche phase delay was correspondingly improved to 80°-85°. In spite of this improved avalanche phase delay the high power efficiency was still poor because of large parasitic resistance in the substrate.

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5. A.K. Gupta, "Fabriation and Characterization of Ion-Implanted n^+p p^+ Silicon Read IMPATT Diodes", Ph.D. Thesis, Cornell University, Ithaca, NY, Jan. 1979.

Personnel Associated with this Task

1. Charles A. Lee, Principal Investigator
2. G. Conrad Dalman, Co-Principal Investigator
3. Aditya Gupta, Graduate Student (Ph.D., January 1979)

G.C. DALMAN and C.A. LEE

5/1/77 - 4/30/79

TITLE: **LARGE SIGNAL MICROWAVE DEVICE-CIRCUIT INTERACTION STUDIES**

Introduction

The research efforts on this task have centered on the development of large signal S-parameters measurement techniques, studies of large signal IMPATT amplifier properties, the development of a 1/2 watt 20 GHz oscillator and large signal studies of FET's. Summaries of the principal results obtained are presented in the following paragraphs.

Large Signal S-Parameter Measurements

Techniques were developed for measuring the S_{11} and S_{22} scattering parameters at large signal levels and are described in a MS thesis published by J. McClymonds.[1] The experimental work was done on IMPATT diodes but the results are applicable to transistors as well. A brief review, extracted from this thesis is as follows:

> *This thesis reports on a new method for* accurately measuring IMPATT admittance and r.f. diode chip voltage amplitude under large signal conditions. The method uses a computer corrected network analyzer with large signal H.P. Network Analyzer.
>
> The small signal admittance of IMPATT diodes can be measured directly with slotted line techniques or with an automatic network analyzer.[2] These measurements are referred to the reference plane of the diode mount, and data at the package or chip reference planes can be found by referring the measured data through an equivalent circuit or bilinear transformation of the mount and package. The equivalent circuit or bilinear transformtion of the mount can be found by solving for the electric and magnetic

fields in the mount,[3,4,5] by replacing the diode with dummy packages of know admittance,[6,7,8] or by biasing the diode to a pre-breakdown voltage and curve-fitting the equivalent circuit to broadband admittance measurements.[9] The equivalent circuit for the package can be found by measuring dummy packages[3,4,5,7,8] or by curve-fitting broadband admittance data.[6,9]

IMPATT diodes must be operated in a cavity when large signal measurements are made so that r.f. voltage harmonics are "shorted out" and only a sinusoidal voltage appears across the diode chip. The difficulties in using a cavity are that the desired diode information must be extracted from data measured outside the cavity and that the admittance seen by the diode must be found. The measurement methods reported in the literature operate diodes in either oscillator or amplifier cavities. If an oscillator circuit is used,[10,11,12] the condition of oscillation $Y_{diode} + Y_{circuit} = 0$ gives Y_{diode} if $Y_{circuit}$ is known. In addition, the equivalent transformer turns ratio between the diode and the measurement plane is needed to calculate the diode r.f. voltage amplitude. If an amplifier circuit is used, a transformation between the diode and the measurement plane outside the cavity must be found.[4,13,14,15] The transformation can be calcualted[4] or the cavity can be modeled by a single-tuned equivalent circuit[13,14,15] and characterized by the perturbation method. The admittance seen by the diode can be measured directly[12,16] or inferred from the equivalent circuit.[4,10,11,13,14,15]

The measurement method presented in this thesis overcomes the difficulties of using a cavity by constructing an amplifier cavity and

diode mount with precision connectors so that the mount can be removed from the cavity. A special calibration method using three offset open circuit calibration standards has been devised so that the computer corrected network analyzer system can be calibrated at the cavity/mount interface. In this way, the effects of the cavity are "calibrated out" along with network analyzer errors so that the corrected data is automatically referred to the mount. Thus the problem of transforming measured data through the cavity is handled automatically by the calibration procedure. The admittance seen by the diode mount is measured directly by connecting a second network analyzer to the cavity. The admittance and r.f. voltage amplitude at the mount plane are referred to the package or chip terminals through an equivalent circuit for the mount and package. The elements of the equivalent circuit are found by curve-fitting the equivalent circuit to small signal, broadband data of the mount and diode when the diode is biased below breakdown.

The body of the thesis is divided into six chapters. Chapter I reviews the operation of network analyzers and how to calibrate them with the use of a computer. Chapter II discusses why IMPATT's should be operated in cavities and what problems are introduced by using cavities. Chapter III explains the calibration method developed for this measurement system to overcome the difficulties introduced by cavities. Chapter IV contains drawings of the special components used in this work together with analyses of their microwave properties. Chapter V outlines the computer programs used

for data analysis. Chapter VI presents and discusses measured data from two IMPATT diodes. The thesis concludes with a discussion of directions for future research.

Large Signal IMPATT Amplifier Properties

Preliminary studies of an 8 GHz reflection amplifier have been studied at large signal levels. Studies of GaAs READ type IMPATT diodes fabricated by Varian Associates and the Raytheon Company have been conducted. Diodes unbedded in a 20 ohm 1/4 wave coaxial circuit yielded 1.65 watts of added power with 2 watts of input power and 12.6% power added conversion efficiency.

Work is under way to improve the gain and an attempt will be made to locate a higher input drive power source. It is anticipated that higher powers can be obtained. Work on constant voltage rather than constant current amplifiers is also in progress.

Methods of determining large-signal diode admittance characteristics from amplifier characteristics have also been developed. Excellent agreement with those found using the large signal H.P. Network Analyzer has been obtained.

Coaxial IMPATT reflection amplifiers using constant voltage[17] bias have been built at X-band which have linear power output versus power input characteristics and low intermodulation distortion. The added power and efficiencies of these amplifiers are comparable to the oscillator results for the same devices. The advantages of using constant voltage bias is that the bias current rises with increasing input power preventing the gain from dropping at high input power levels. The best amplifier thus far has a maximum C.W. output power of 6.0 watts, 3.1 dB gain and a corresponding third order intermodulation of -14 dB, neglecting circulator losses.

Admittance measurements as a function of r.f. input power were also made on these amplifiers using a high power automatic network analyzer. This data is used to find the chip conductance and susceptance as a function of chip r.f. voltage. This data has contributed to an understanding of the origin of intermodulation

distortion in linear amplifier applications.

Constant voltage amplifiers such as these could be a very attractive alternative to the travelling wave amplifier in communication systems.

Work at 20 GHz is also under way. Two 560 mW oscillators operating with 12.7% efficiency were fabricated using Varian GaAs IMPATTs in a hat-structure waveguide circuit. Amplifier studies will be conducted using a modified version of these oscillators.

Large Signal Studies of FET's

Preliminary experimental studies were carried out on microwave FET's. Measurements were carried out at small and large signal levels on medium power and low power Microwave Semiconductor Company devices over a range of frequencies from 3.0 to 7.5 GHz using a WATs test fixture and an experimental MSC amplifier circuit. The results obtained on type MSC 88001 low power transistors showed that S_{11}, S_{21} and S_{22} are independent of drive levels up to the point at which gate current is drawn. The MSC 88002 medium power transistor results also showed that S_{22} is independent of drive but both S_{11} and S_{21} are drive sensitive. A power added gain of 3 dB was obtained at 5.9 GHz with an input power level of 0.1 watts. S_{21} of 0 dB was obtained at a drive level of 0.4 watts.

Further studies, including intermodulation studies, will be made at very large signal levels.

Personnel Associated Under This Task

1. G. C. Dalman, Principal Investigator
2. C. A. Lee, Co-Principal Investigator
3. J. McClymonds - Graduate Student (M.S. Thesis 6/78)
4. H. Kondoh, Graduate Student

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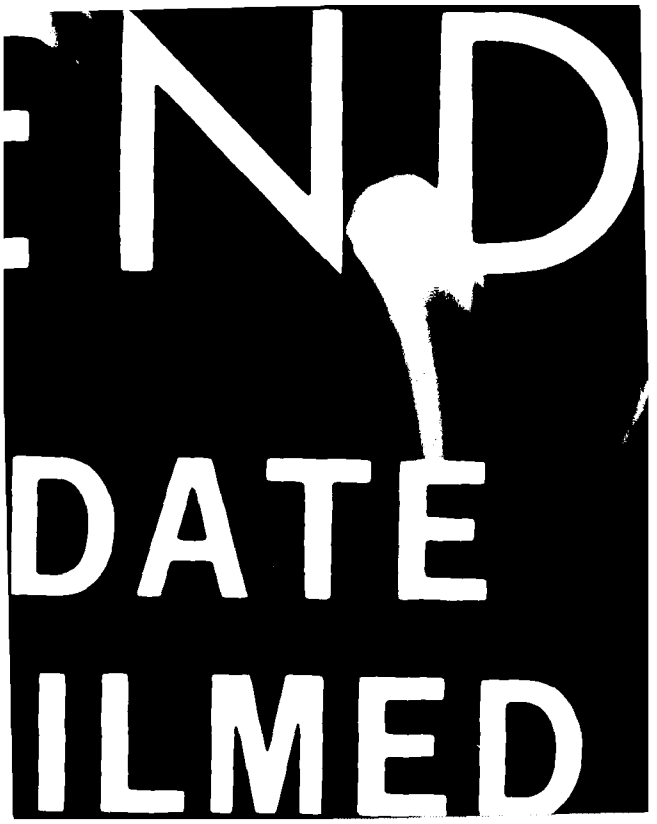
List of Papers Presented

17. "Linear High Power IMPATT Amplifiers Using Constant Voltage Bias", J.W. McClymonds, G.C. Dalman and C.A. Lee, presented at 7th Biennial Conference on Active Microwave Semiconductor Devices and circuits, Cornell University, Ithaca, NY, August 14-16, 1979.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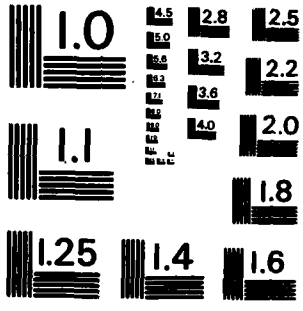

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The growth and characterization of high purity and chromium doped GaAs a Al,GaAs for buffer layers in high performance GaAs FET's has been carried out Deep level transient spectroscopy has been used to measure electron traps in Schottky diodes and GaAs FET's.

The investigation of microwave field-effect transistor performance limit set by layer composition and contact geometry has been carried out. The

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several critical physical electronics parameters for very high voltage operation of GaAs power FET's have been determined. The electric field distribution and the parasitic output conductance due to buffer layer current were studied and optimized.

The use of MBE tailored doping profiles for improved microwave device operation has been studied. Improved linearity of GaAs power FET devices and the optimization of doping planes for potential barriers and other purposes were also carried out.

GaAs/Al,GaAs selectively doped heterojunctions were grown by MBE and were studied for potential use in high performance transistors. High electron mobility (80.000 $cm^2/v\text{-}s$) at 77^oK was first obtained in this effort, following the optimization of the growth conditions of the Al,GaAs. In addition, high resistivity Al,GaAs buffer layers for power FET's were obtained.

Two dimensional computer simulations of FET devices in various materials were also made. Some techniques for reducing leakage in Schottky barriers on low-band-gap material were investigated.

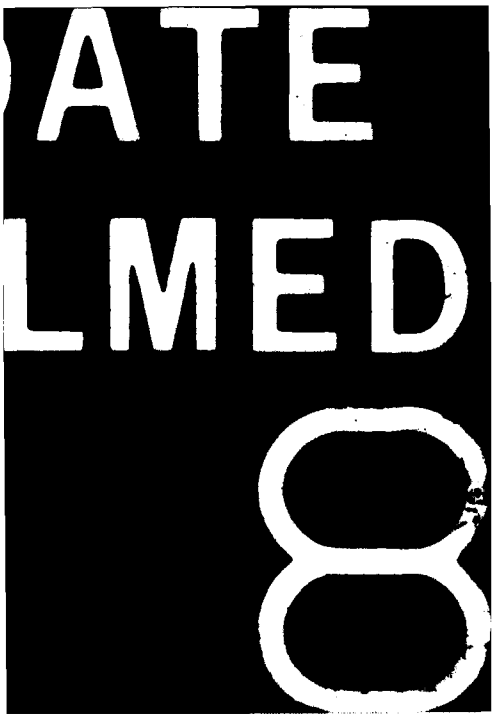
Fundamental design studies for GaAs FET integrated circuits were carried out using a computer. Matching networks for optimisized gain or noise figures, across bread bands, were determined.

A new method of broadband circuit design which does not require device equivalent circuit determination, has also been studied, and some particular examples have been optimized.

The dynamic and spectral characteristics of semiconductor laser materials and structures have been investigated. Several specific laser systems, including external components are included.

High speed optical receivers for optical communications were investigated. New high speed detectors using GaAs and In,GaAs were constructed and tested.

A project to construct MOCVD equipment for compound semiconductor growth has also been underway, in order to complement the MBE and LPE methods already developed.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